

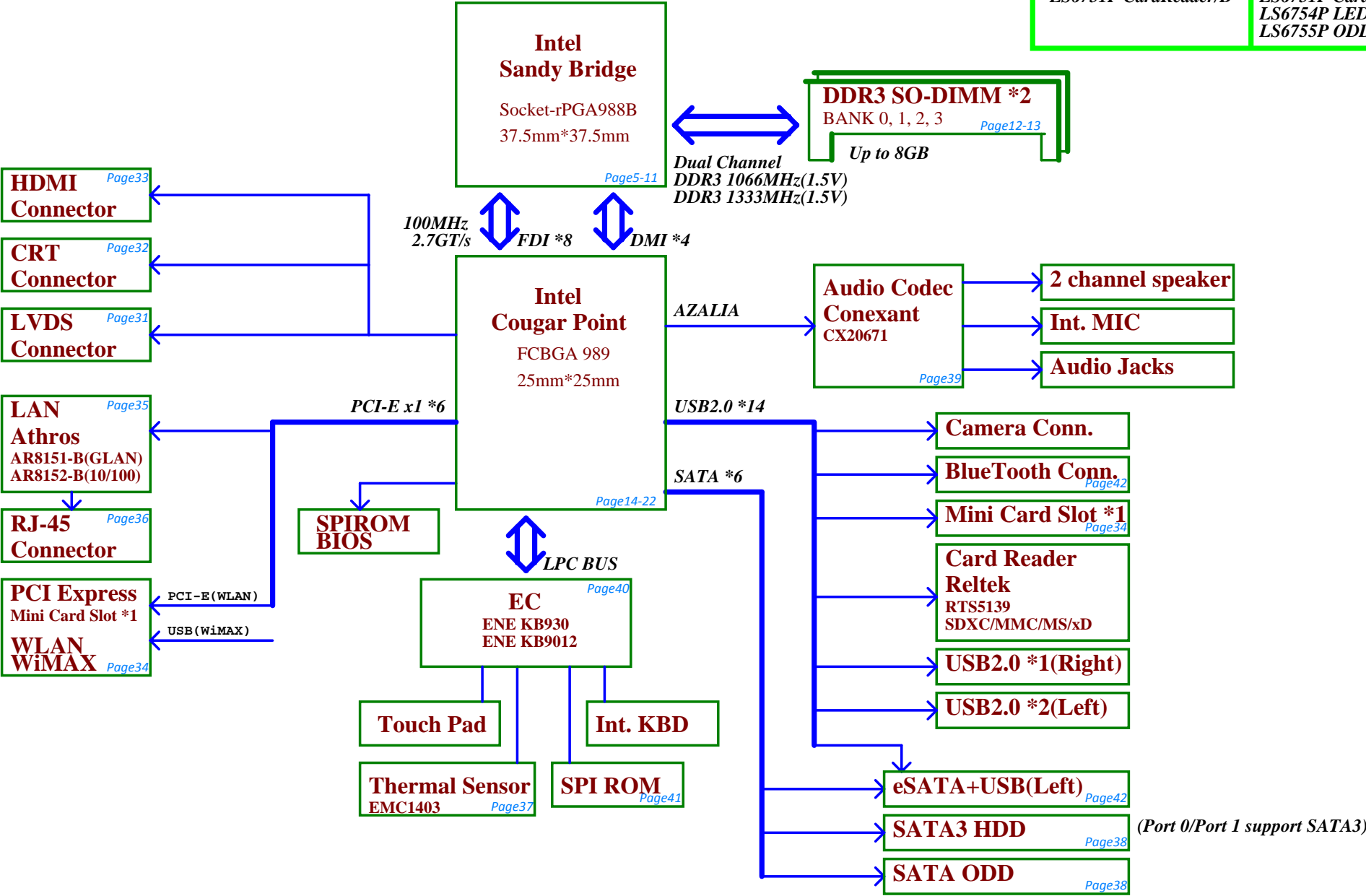
**Compal Confidential**  
**G470/G570 UMA M/B Schematics Document**  
**Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH**

**2010-12-03**  
**LA-675AP**  
**REV:1.0**

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For 14"(Page 4x)  
LS6753P PWR/B  
LS6751P CardReader/B

For 15"(Page 4x+1)  
LS6753P PWR/B  
LS6751P CardReader/B  
LS6754P LED/B  
LS6755P ODD/B



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## Voltage Rails

power plane	State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +0.75VS +1.05VS
S0					
S3					
S5 S4/AC					
S5 S4/ Battery only					
S5 S4/AC & Battery don't exist					

Address

### EC SM Bus1 address

### EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Thermal Sensor EMC1403-2	1001_101xb

### PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

## SMBUS Control Table

	SOURCE	VGA	BATT	KE930	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1	KB930	X	V	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW					
SMB_EC_CK2	KB930	X	X	X	X	X	X	V
SMB_EC_DA2	+3VALW							+3VS
SMBCLK	PCH	X	X	X	V	V	X	X
SMBDATA	+3VALW				+3VS	+3VS		
SML0CLK	PCH	X	X	X	X	X	X	X
SML0DATA	+3VALW							
SML1CLK	PCH	V	X	V	X	X	V	X
SML1DATA	+3VALW	+3VS		+3VS			+3VS	

## BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

## USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB Port (Left Side)
	UHCI1	2	USB Port (Left Side)
		3	USB Port (Left Side)
	UHCI2	4	
		5	Camera
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Mini Card(WLAN)
		9	
	UHCI5	10	
		11	Card Reader
	UHCI6	12	
		13	Blue Tooth

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra/Rc/Re	100K +/- 5%				
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max	
0	0	0 V	0 V	0 V	EVT
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	DVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	PVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	MP
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	2.500 V	3.300 V	3.300 V	

## BOM Structure Table

BTO Item	BOM Structure
CAMERA DEVICE	CMOS@
Blue Tooth	BT@
eSATA	ESATA@
COMMON HDMI	HDMI@
Connector	ME@
45 LEVEL	45@
10/100 LAN	8152@
GIGA LAN	GIGA@
Unpop	@

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				Size B	Document Number LA-675AP	Rev 1.0
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Power-Up/Down Sequence

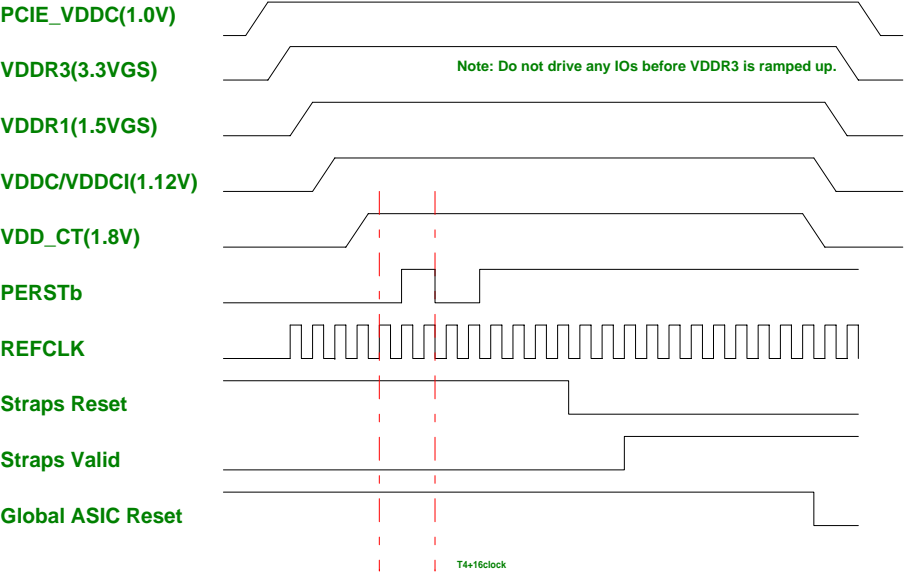
All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.

VDDR3 should ramp-up before or simultaneously with VDDC.

For LVDS, DPx\_VDD10 should ramp-up before DPx\_VDD18 and the PCIe Reference clock should begin before DPx\_VDD18. For power-down, DPx\_VDD18 should ramp-down before DPx\_VDD10.

The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD\_CT have ramped up.

VDDC and VDD\_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD\_CT starts to ramp-up (or vice versa).)



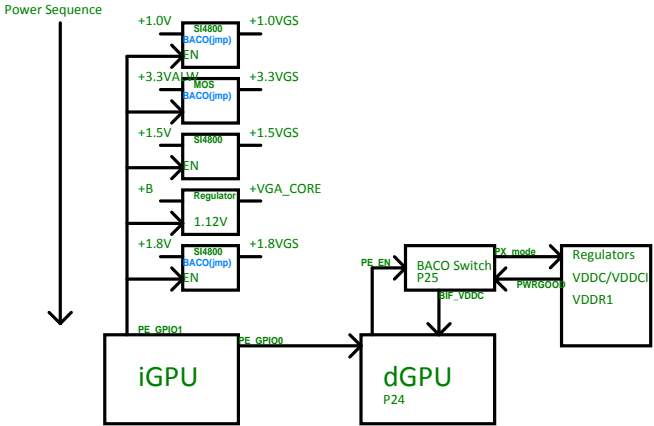
Without BACO option :

- PE\_GPIO0 : Low -> Reset dGPU ; High ->Normal operation
- PE\_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

BACO option :

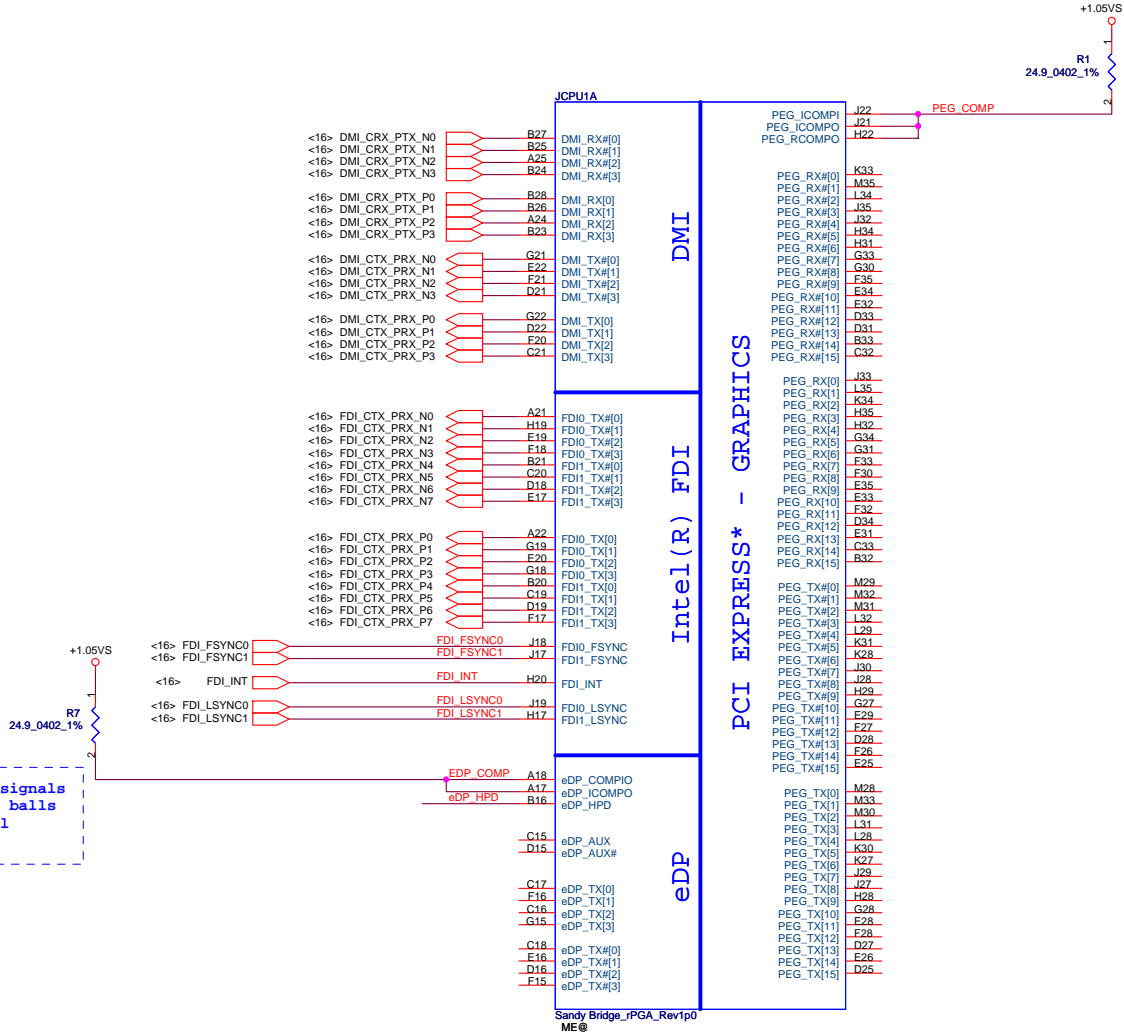
- PE\_GPIO0 : High ->Normal operation (dGPU is not reseton BACO mode)
- PE\_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

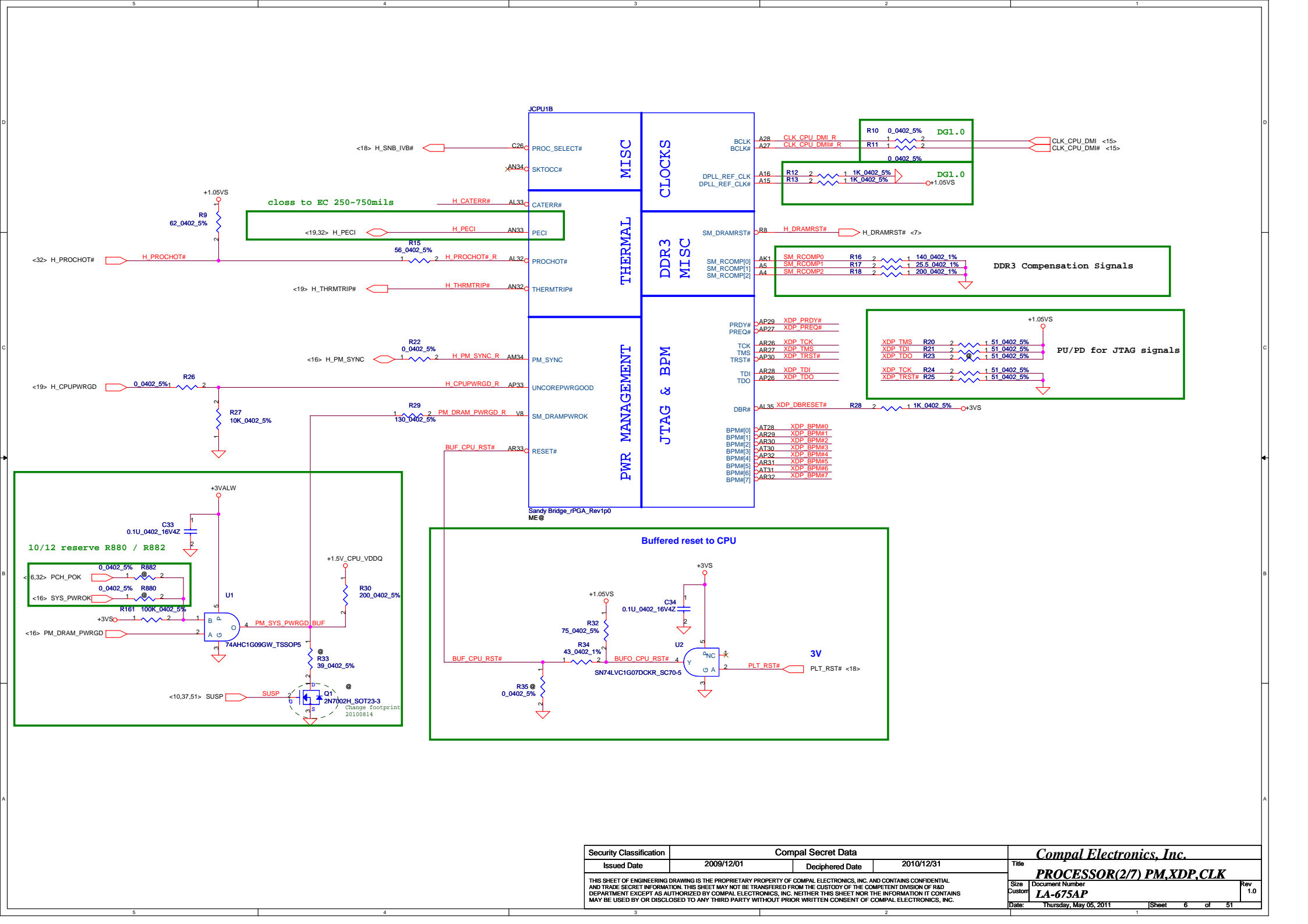
dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIe_PVDD, PCIe_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIe_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIe_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A

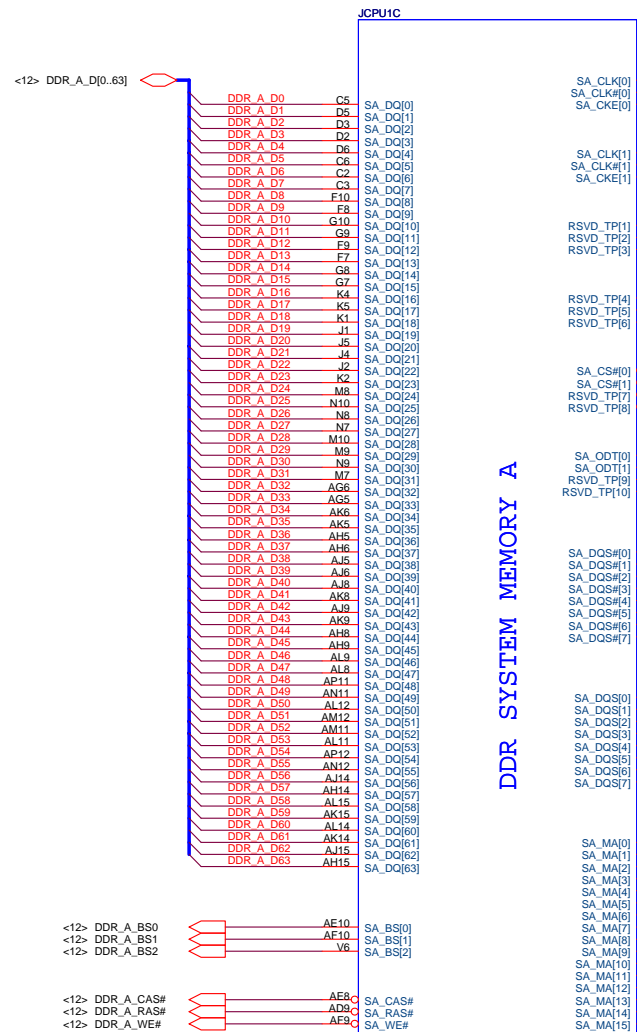


eDP\_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

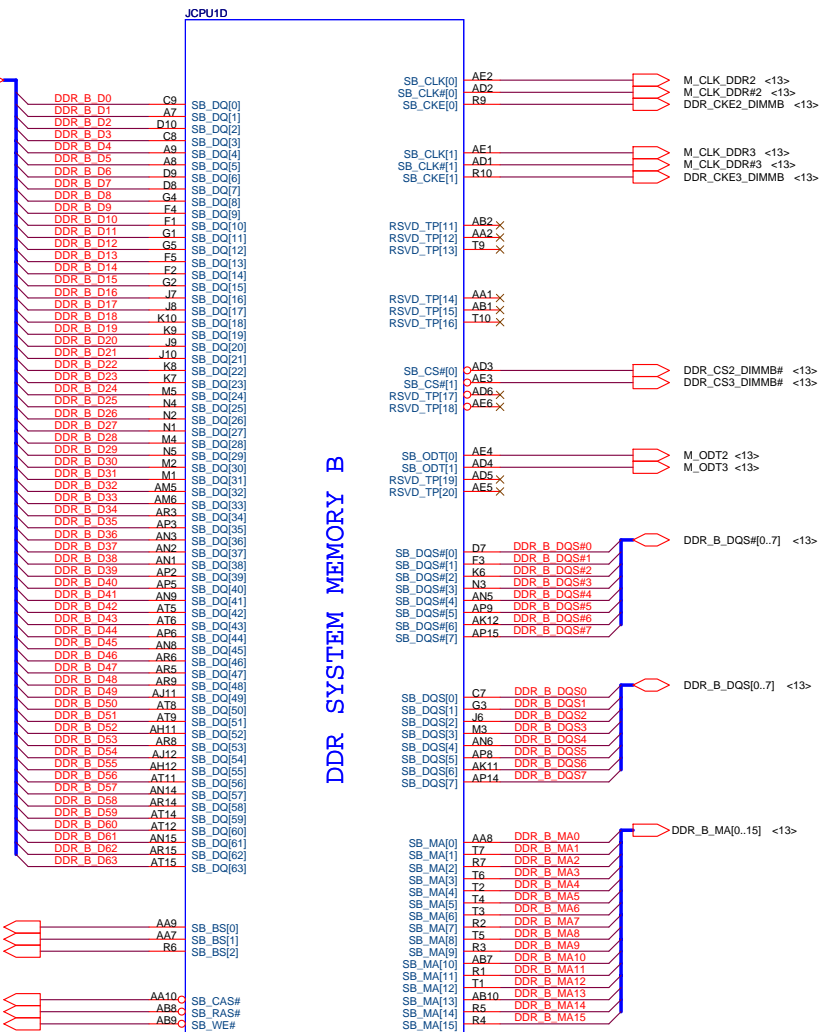
PEG\_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms  
PEG\_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms







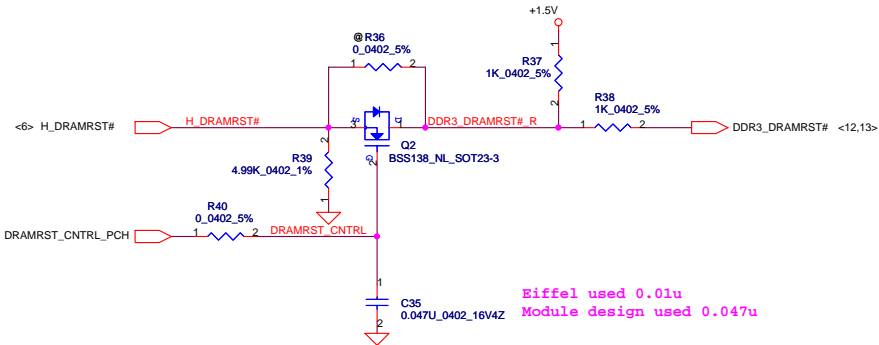
DDR SYSTEM MEMORY A



DDR SYSTEM MEMORY B

Sandy Bridge\_rPGA\_Rev1p0  
ME @

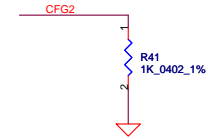
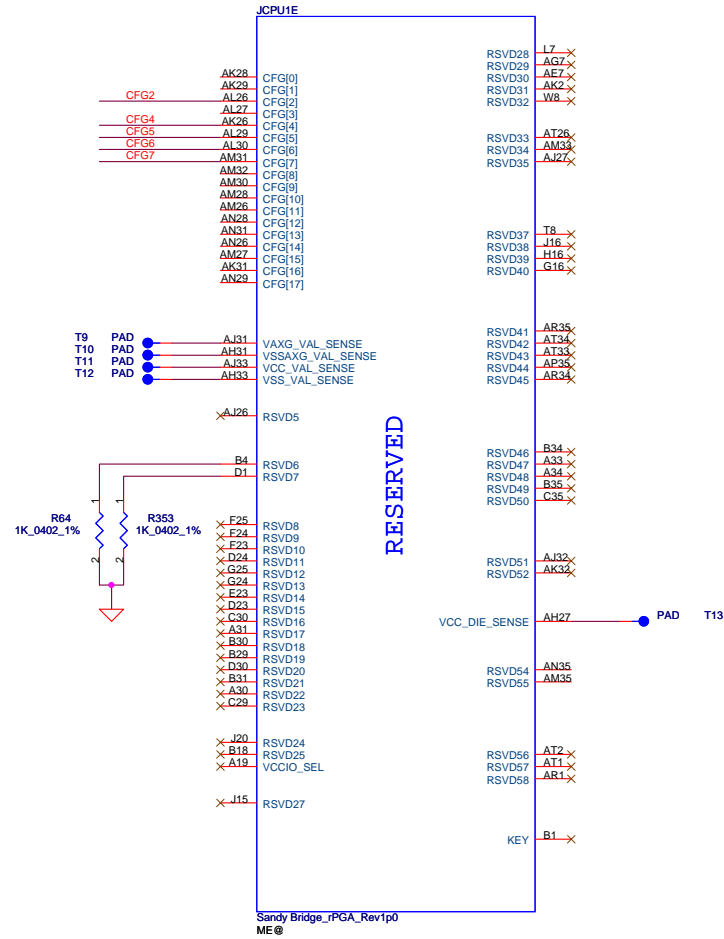
Sandy Bridge\_rPGA\_Rev1p0  
ME @



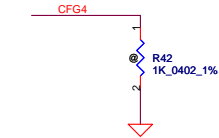
Eiffel used 0.01u  
Module design used 0.047u

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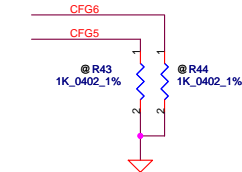
## CFG Straps for Processor



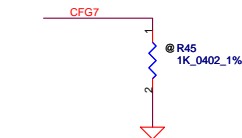
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

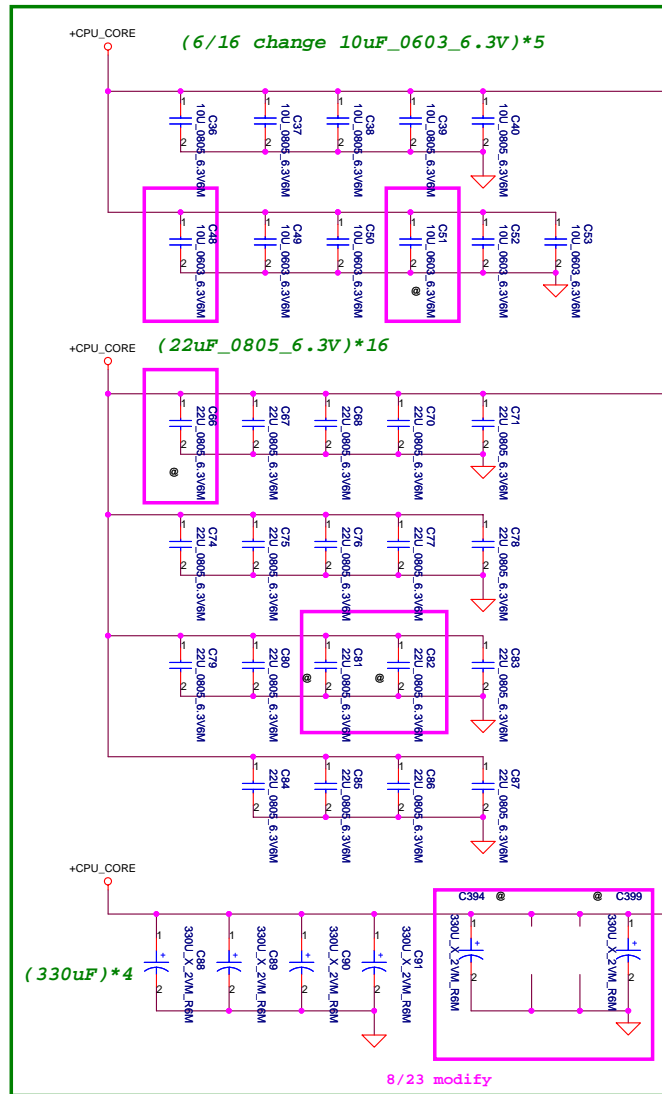


PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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								PROCESSOR(4/7) RSVD,CFG	
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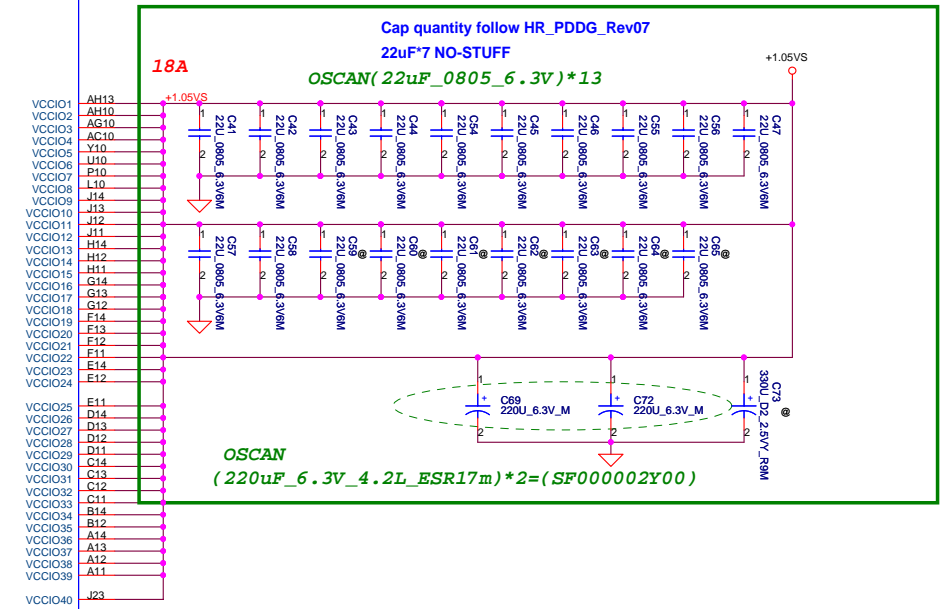


QC=94A  
DC=53A

- JCPU1F
- AG35 VCC1
  - AG34 VCC2
  - AG33 VCC3
  - AG32 VCC4
  - AG31 VCC5
  - AG30 VCC6
  - AG29 VCC7
  - AG28 VCC8
  - AG27 VCC9
  - AG26 VCC10
  - AF35 VCC11
  - AF34 VCC12
  - AF33 VCC13
  - AF32 VCC14
  - AF31 VCC15
  - AF30 VCC16
  - AF29 VCC17
  - AF28 VCC18
  - AF27 VCC19
  - AF26 VCC20
  - AD35 VCC21
  - AD34 VCC22
  - AD33 VCC23
  - AD32 VCC24
  - AD31 VCC25
  - AD30 VCC26
  - AD29 VCC27
  - AD28 VCC28
  - AD27 VCC29
  - AD26 VCC30
  - AC35 VCC31
  - AC34 VCC32
  - AC33 VCC33
  - AC32 VCC34
  - AC31 VCC35
  - AC30 VCC36
  - AC29 VCC37
  - AC28 VCC38
  - AC27 VCC39
  - AC26 VCC40
  - AA35 VCC41
  - AA34 VCC42
  - AA33 VCC43
  - AA32 VCC44
  - AA31 VCC45
  - AA30 VCC46
  - AA29 VCC47
  - AA28 VCC48
  - AA27 VCC49
  - AA26 VCC50
  - Y35 VCC51
  - Y34 VCC52
  - Y33 VCC53
  - Y32 VCC54
  - Y31 VCC55
  - Y30 VCC56
  - Y29 VCC57
  - Y28 VCC58
  - Y27 VCC59
  - Y26 VCC60
  - Y25 VCC61
  - Y24 VCC62
  - Y23 VCC63
  - Y22 VCC64
  - V31 VCC65
  - V30 VCC66
  - V29 VCC67
  - V28 VCC68
  - V27 VCC69
  - V26 VCC70
  - U35 VCC71
  - U34 VCC72
  - U33 VCC73
  - U32 VCC74
  - U31 VCC75
  - U30 VCC76
  - U29 VCC77
  - U28 VCC78
  - U27 VCC79
  - U26 VCC80
  - R35 VCC81
  - R34 VCC82
  - R33 VCC83
  - R32 VCC84
  - R31 VCC85
  - R30 VCC86
  - R29 VCC87
  - R28 VCC88
  - R27 VCC89
  - R26 VCC90
  - P35 VCC91
  - P34 VCC92
  - P33 VCC93
  - P32 VCC94
  - P31 VCC95
  - P30 VCC96
  - P29 VCC97
  - P28 VCC98
  - P27 VCC99
  - P26 VCC100

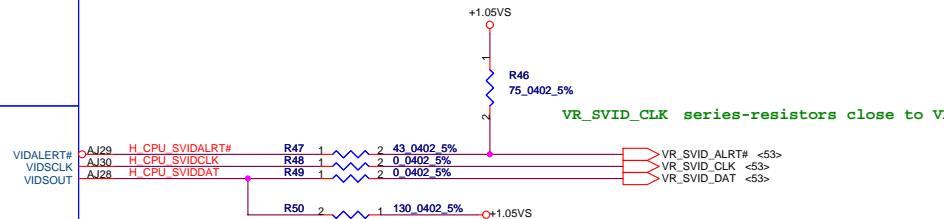
## POWER

### PEG AND DDR

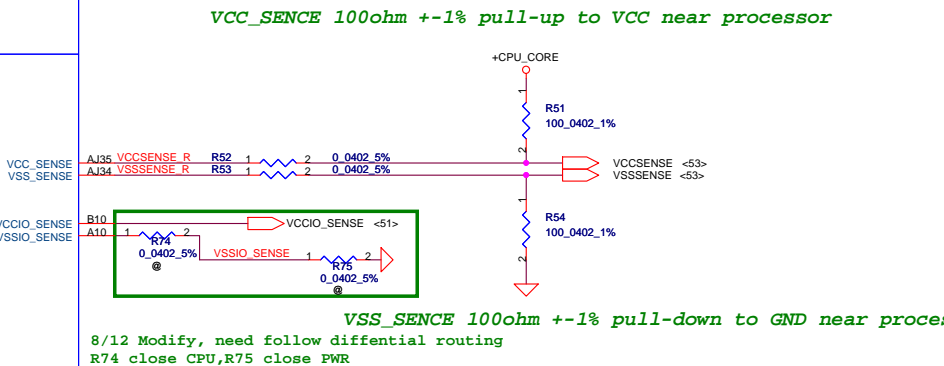


## CORE SUPPLY

### SVID



### SENSE LINES

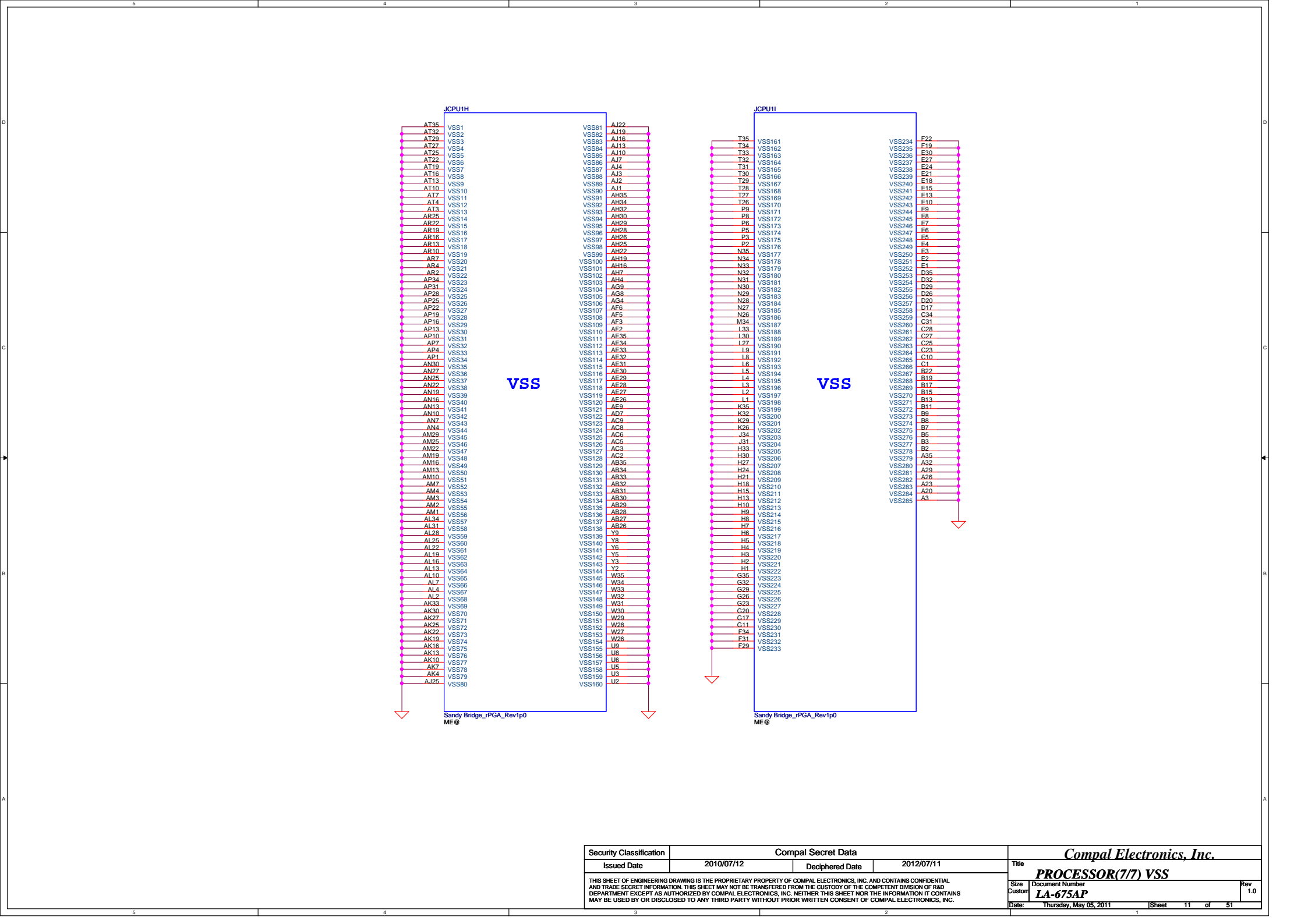


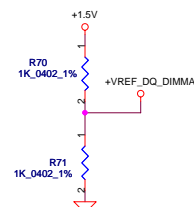
Sandy Bridge\_rPGA\_Rev100  
ME@

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PROCESSOR(5/7) PWR,BYPASS		
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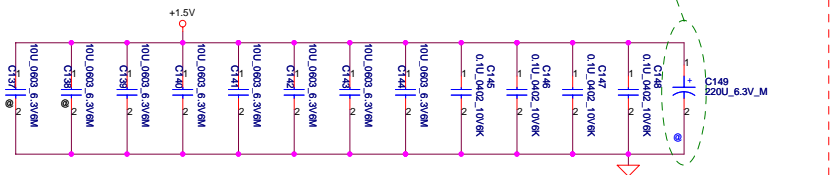




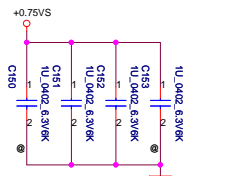
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OSCAN (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)
(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4

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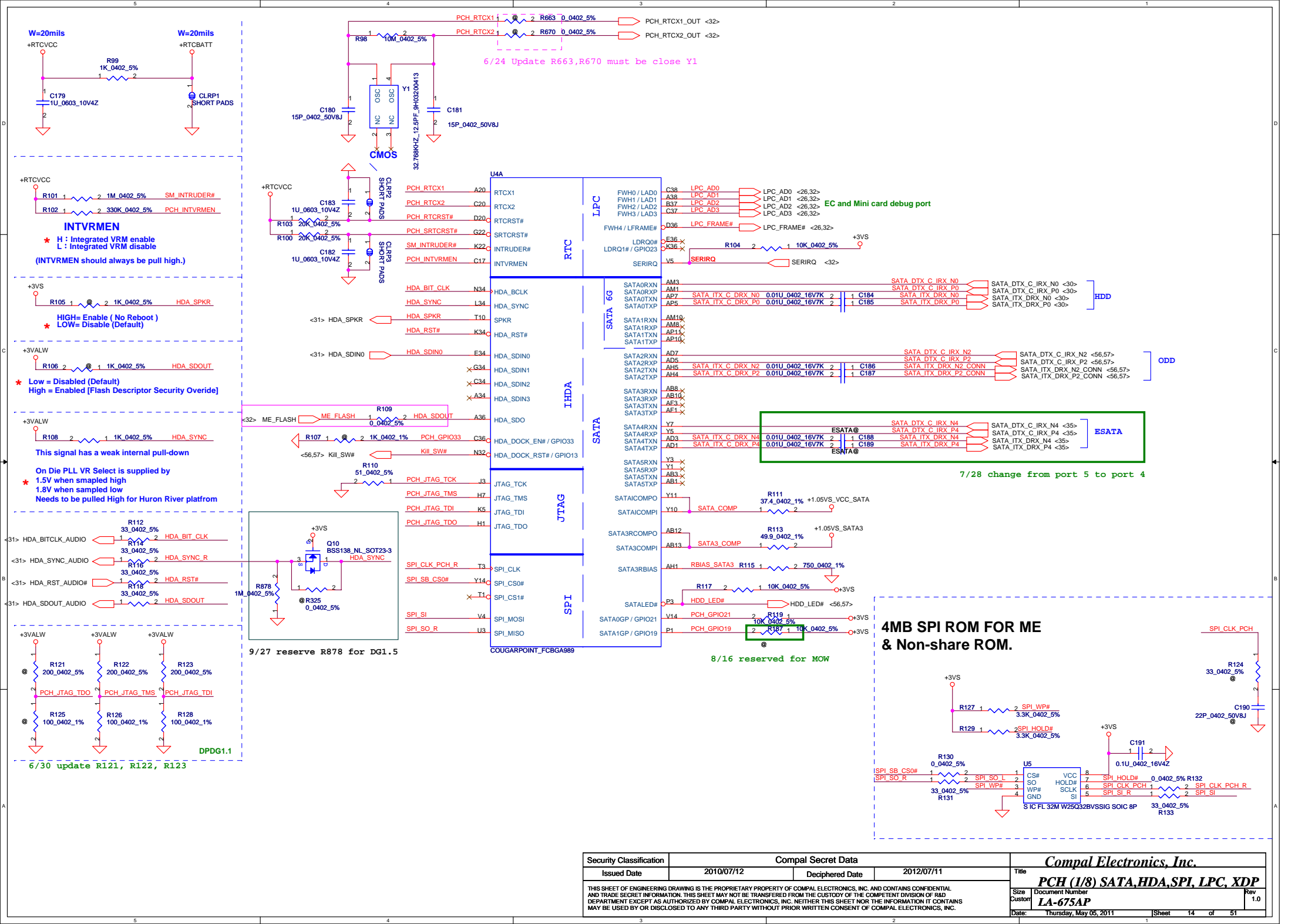
7/28 Update connect GND directly

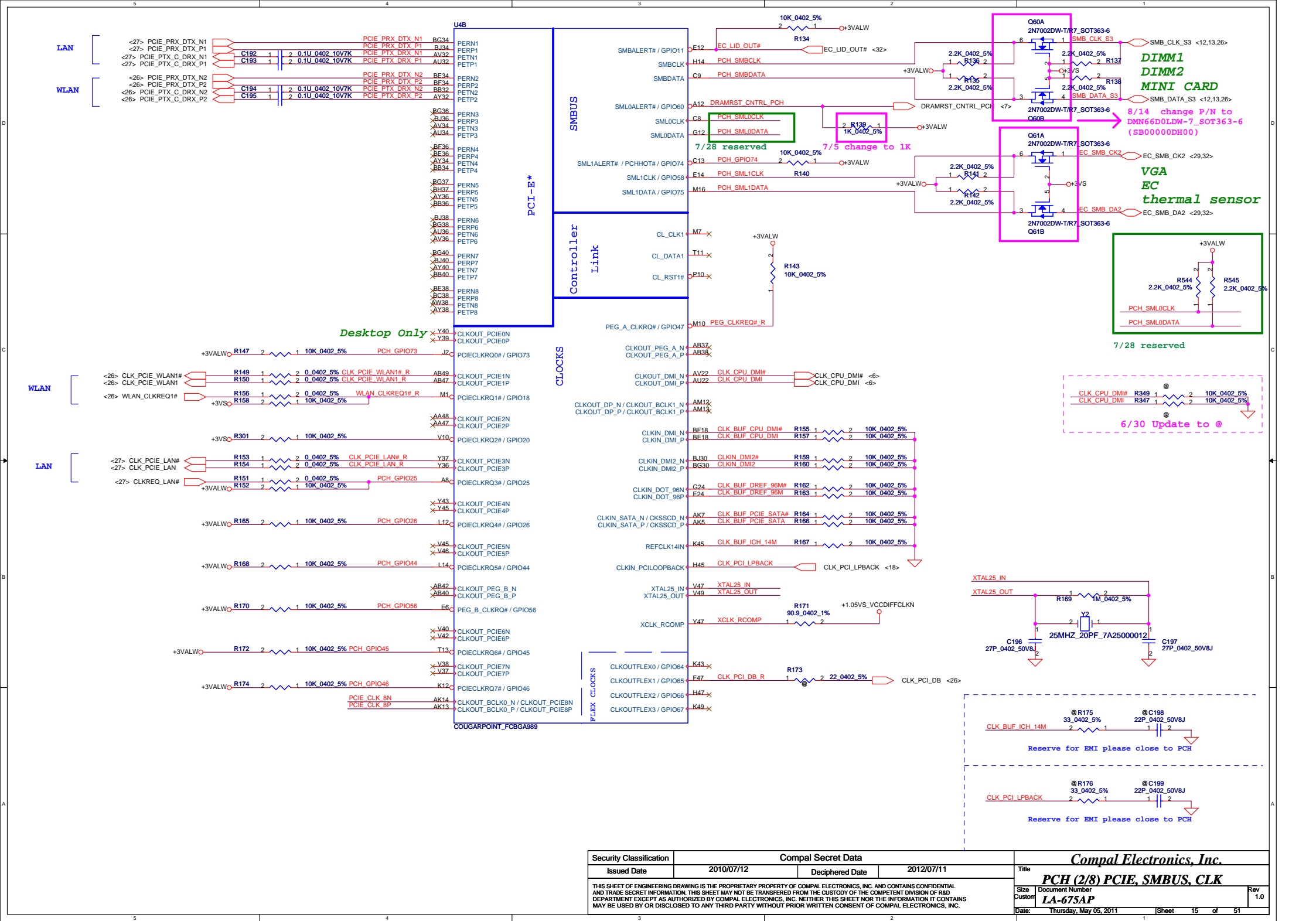


**Layout Note:**  
Place near DIMM

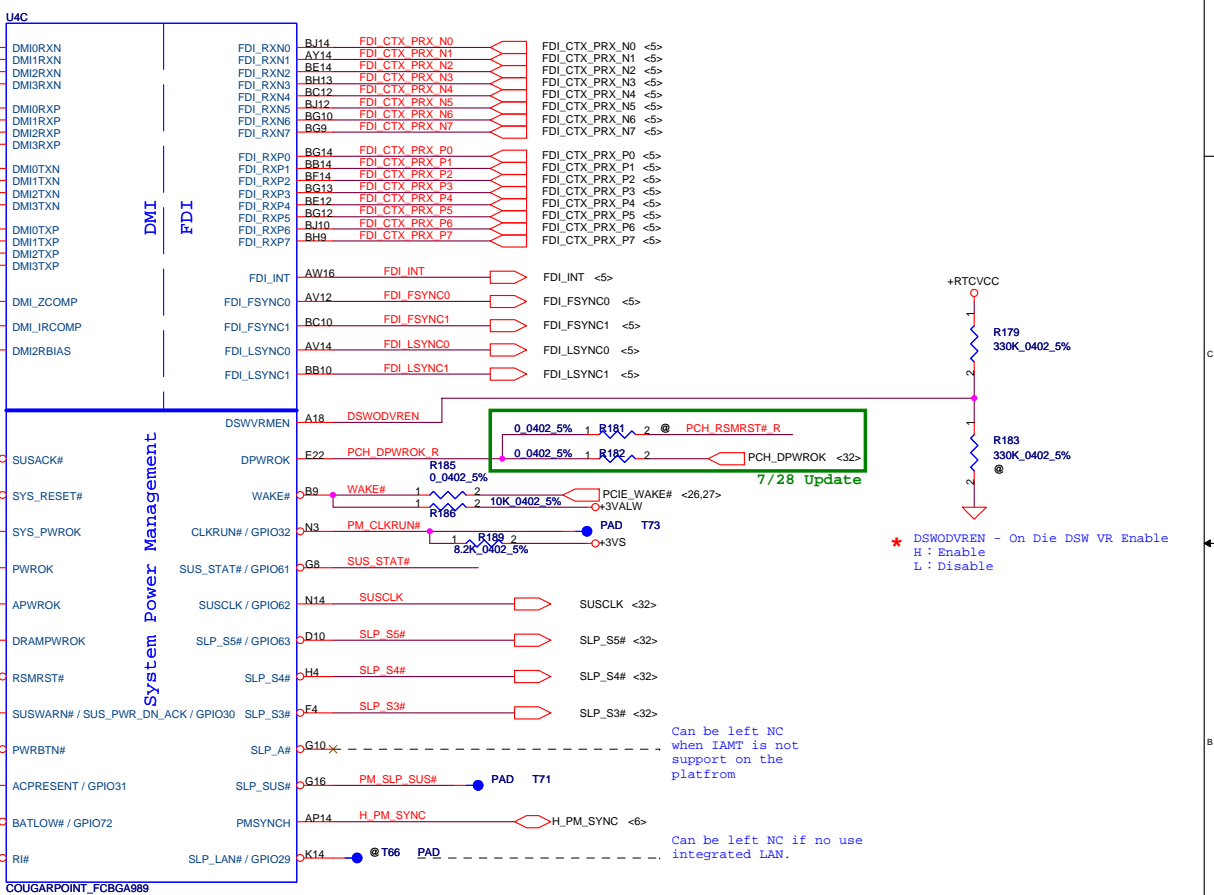
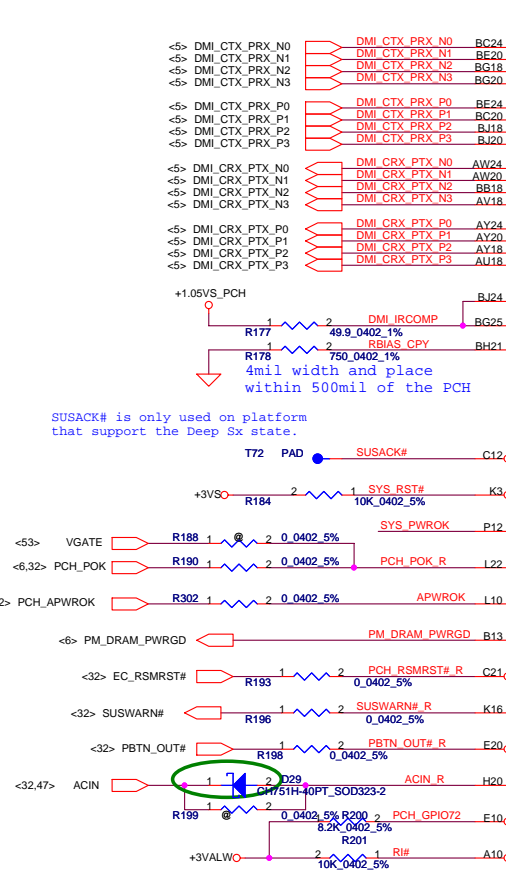
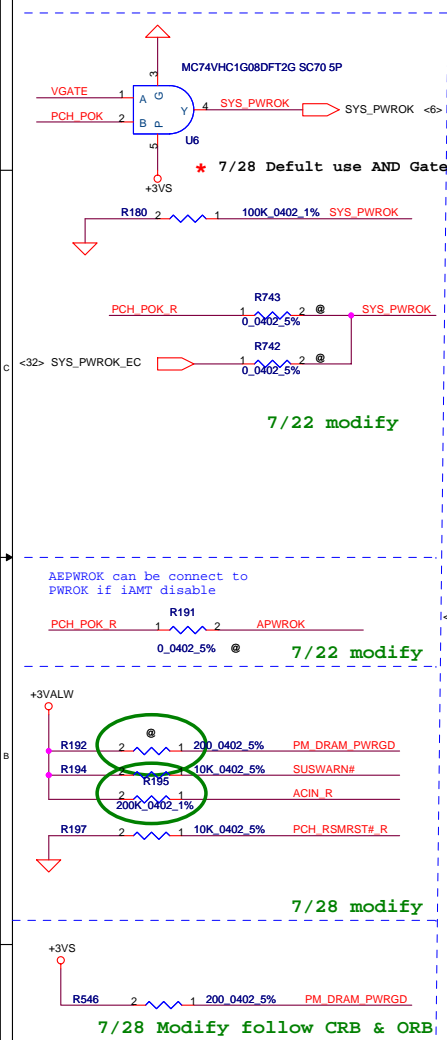
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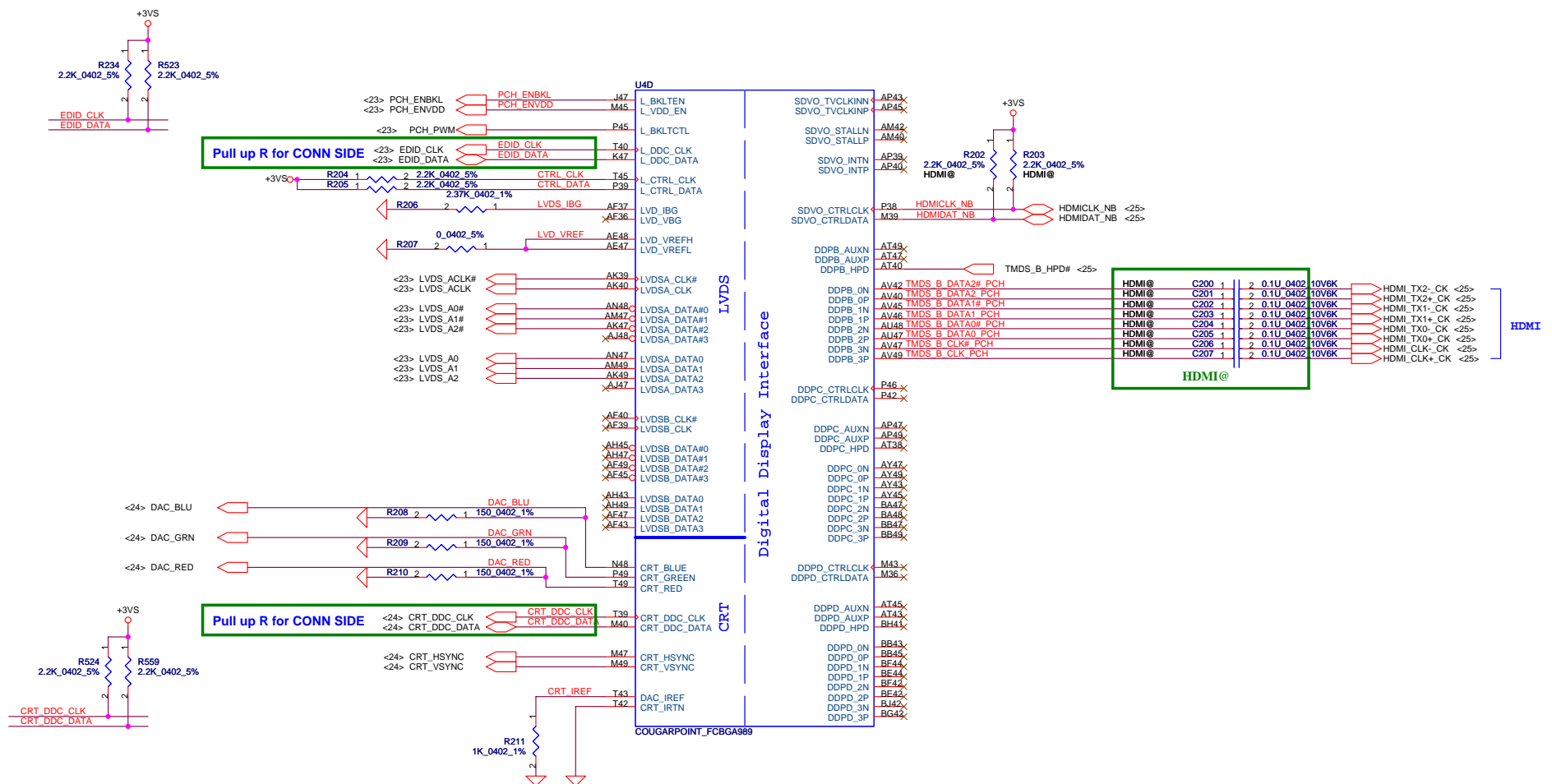






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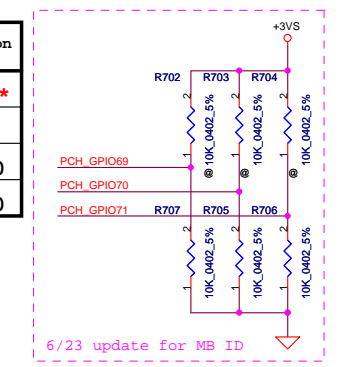
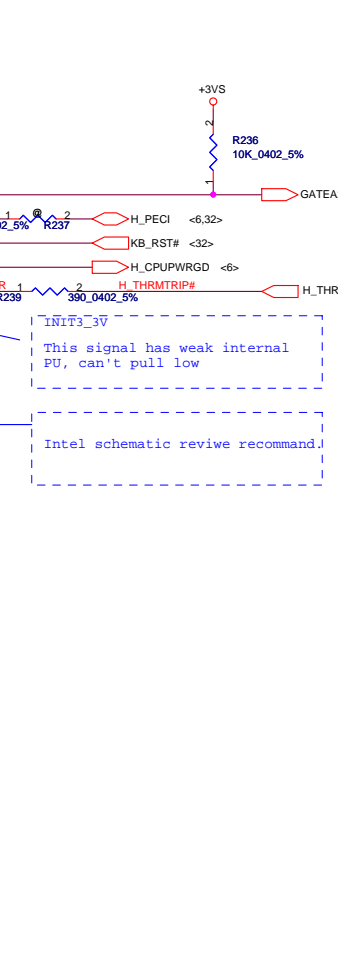
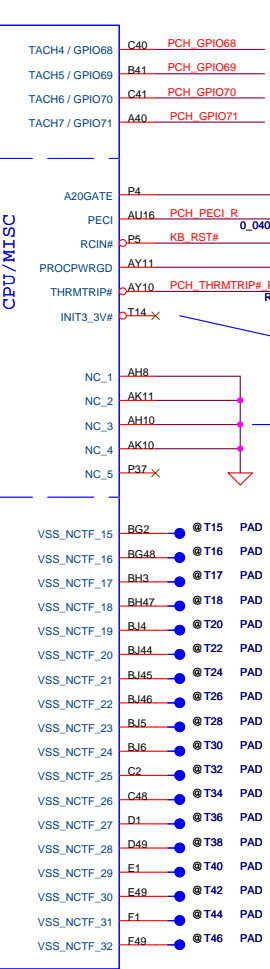
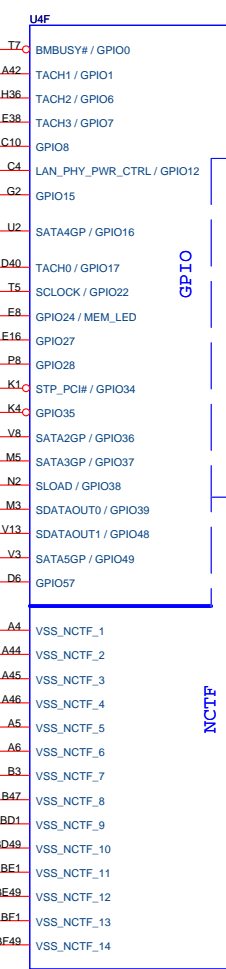
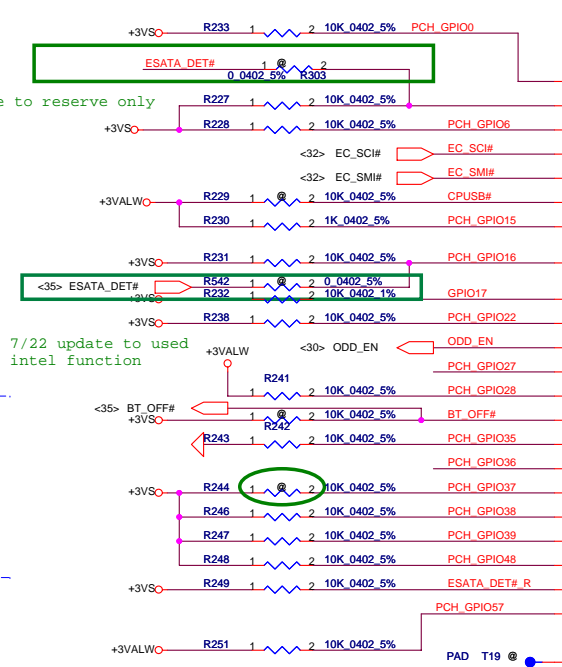
ICC\_EN#  
Integrated Clock Chip Enable  
H : Disable  
L : Enable  
★ H : Disable  
L : Enable  
7/22 update to reserve only  
R235 1 2 1K 0402 5% EC\_SMI#  
Weak internal pull-high

GPIO28  
On-Die PLL Voltage Regulator  
This signal has a weak internal pull up  
★ H : On-Die voltage regulator enable  
L : On-Die PLL Voltage Regulator disable  
R240 1 2 1K 0402 5% PCH\_GPIO28

PCH\_GPIO27 (Have internal Pull-High)  
★ High: VCCVRM VR Enable  
Low: VCCVRM VR Disable  
R245 1 2 1K 0402 5% PCH\_GPIO27

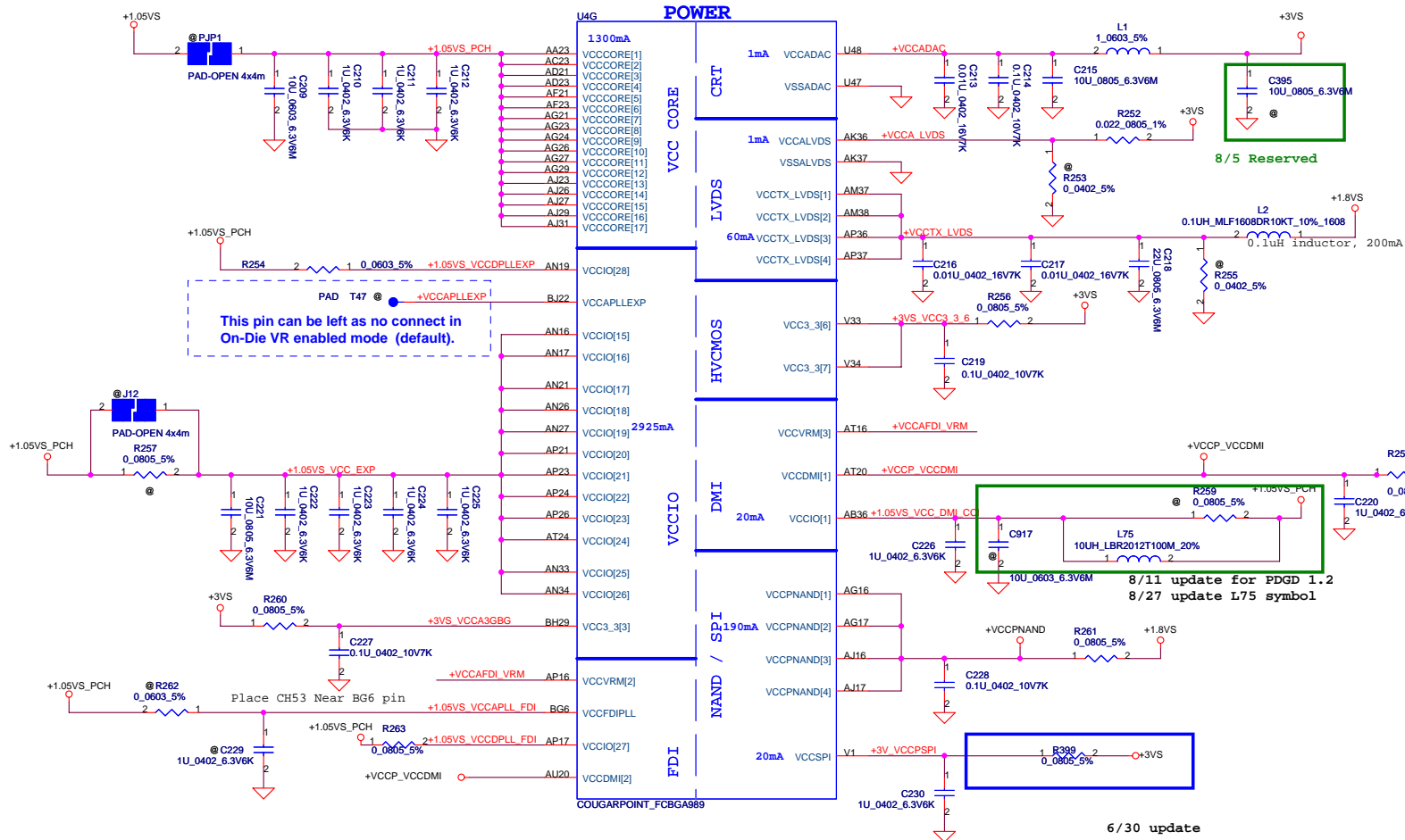
+3VS R250 1 2 1K 0402 5% PCH\_GPIO36  
R547 1 2 1K 0402 5%  
8/5 update to pull down

R881 1 2 1K 0402 5% PCH\_GPIO37  
10/8 update to pull down for checklist Rev1.2



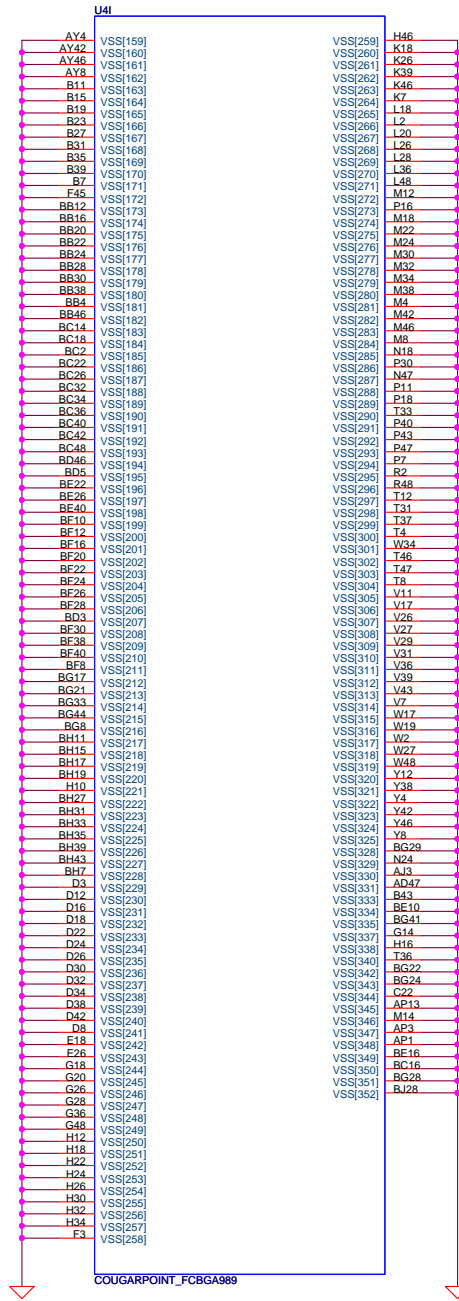
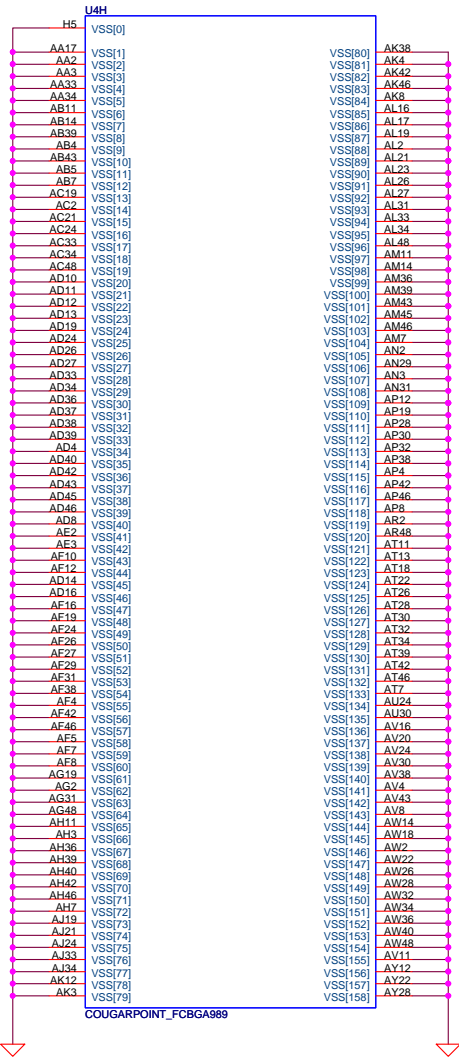
PCH_GPIO69	PCH_GPIO70	PCH_GPIO71	Function
0	0	0	UMA *
1	0	0	DIS
0	1	0	PX3.0
1	1	0	PX4.0

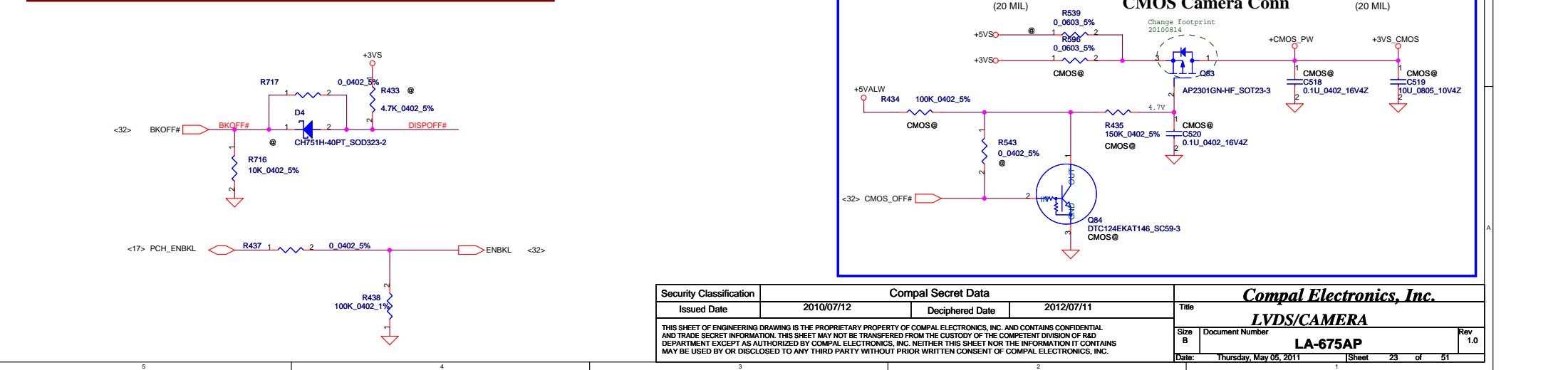
COUGARPOINT\_FCBGA989



PCH Power Rail Table		
Voltage Rail	Voltage	60 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccLVDS	3.3	0.001
VccTX_LVDS	1.8	0.06







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Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title	
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					<b>LA-675AP</b> Date: Thursday, May 05, 2011   Sheet 23 of 51
				Rev	1.0

UMA only

<17> DAC\_RED  
<17> DAC\_GRN  
<17> DAC\_BLU

8/6 Modify,

CLOSE TO CONN

<17> CRT\_HSYNC

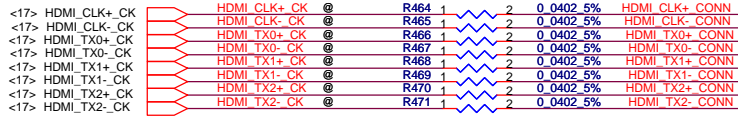
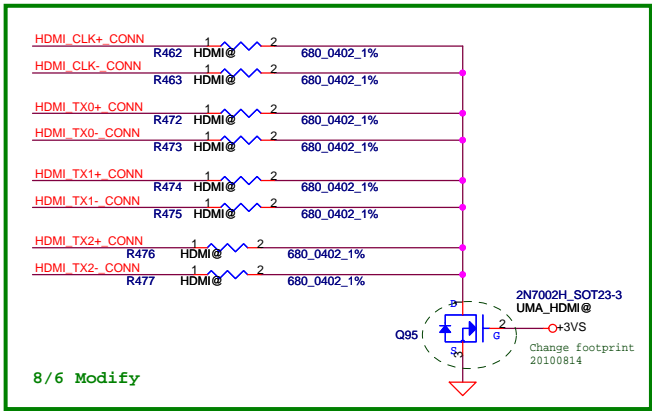
<17> CRT\_VSYNC

<17> CRT\_DDC\_DATA

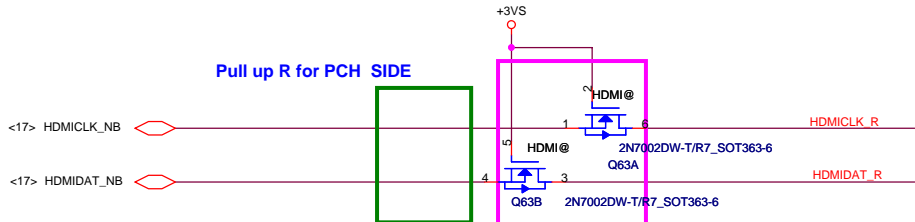
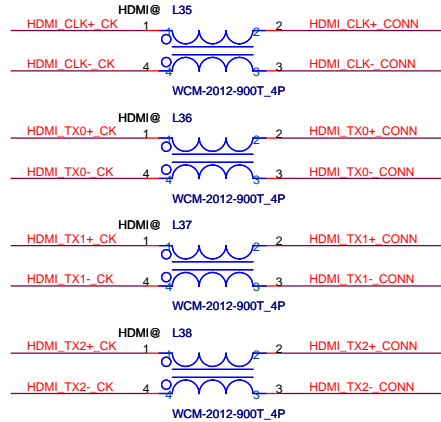
<17> CRT\_DDC\_CLK

8/14 change P/N to  
DMN66D0LDW-7\_SOT363-6  
(SB00000DH00)

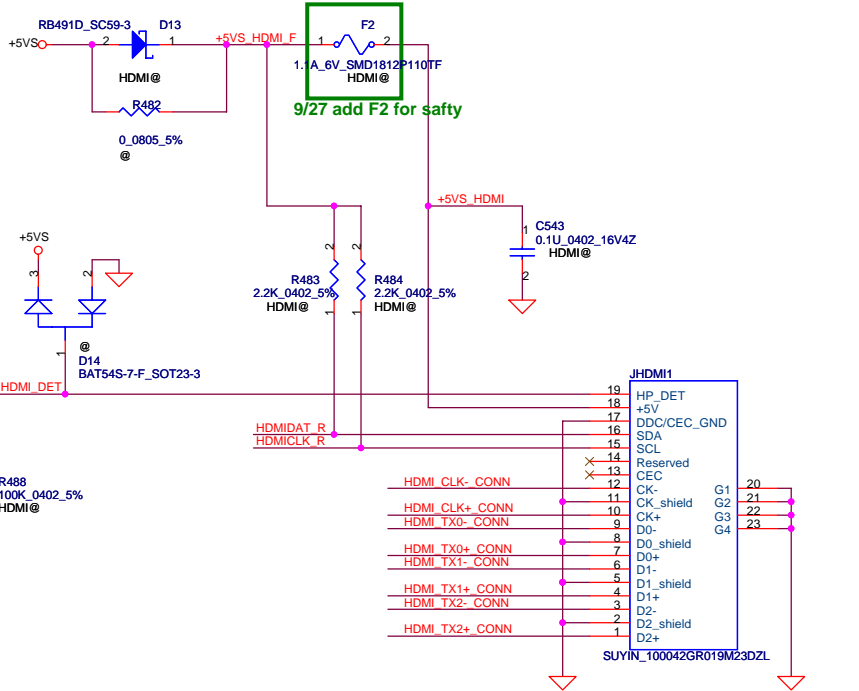
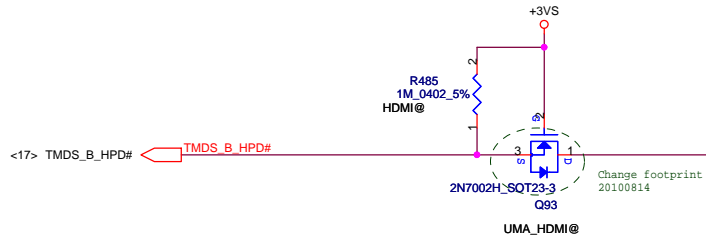
Security Classification		Compal Secret Data				<b>Compal Electronics, Inc.</b>			
Issued Date		2010/07/12		Deciphered Date		2012/07/11		Title	
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						Size	Document Number		Rev
						Custom	LA-675AP		1.0
Date:		Thursday, May 05, 2011				Sheet		24	of 51



12/02 change L35-L38 P/N to SM070000I00

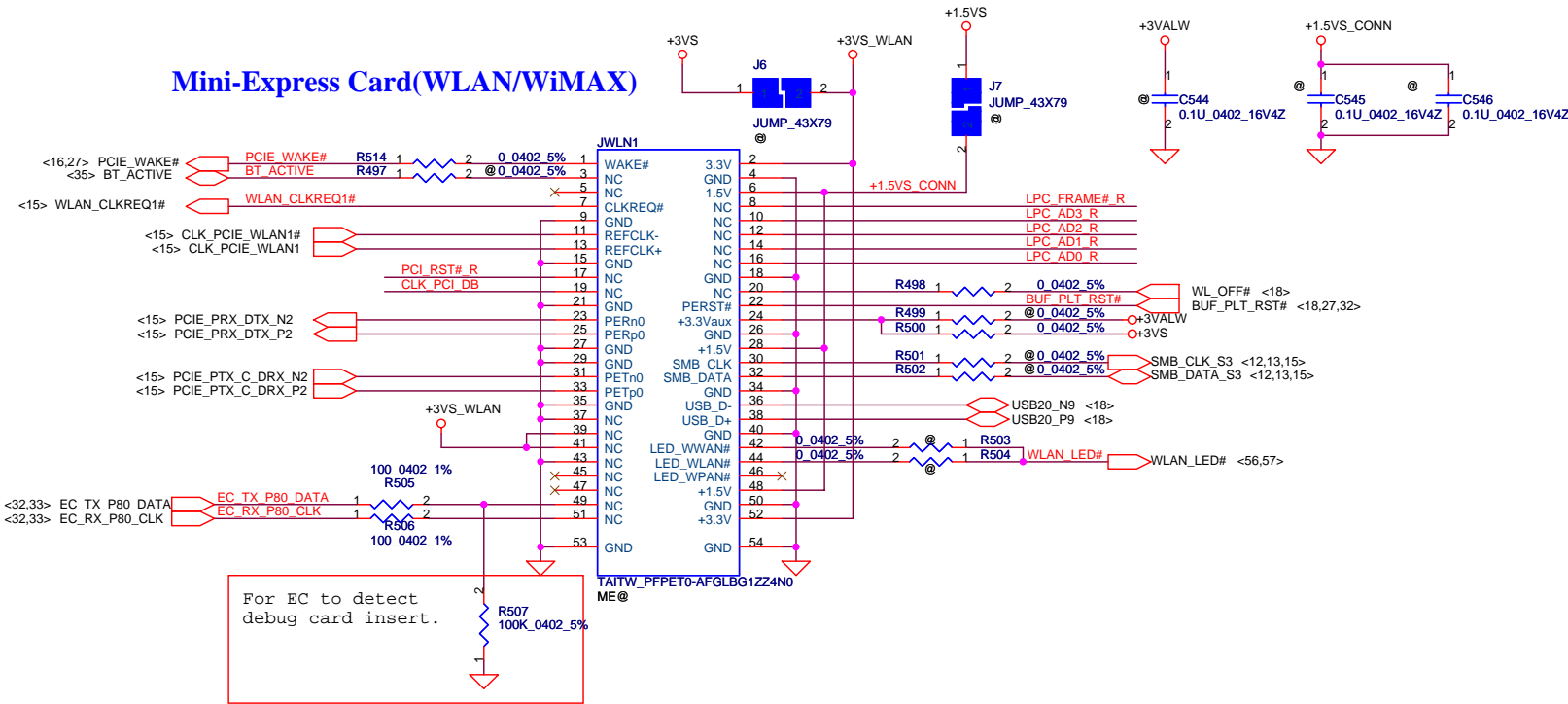


8/14 change P/N to DMN66D0LDW-7\_SOT363-6 (SB00000DBH00)



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Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title	
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Size	Custom	Document Number	LA-675AP	Rev	1.0
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Mini-Express Card for WLAN/WiMAX(Half)



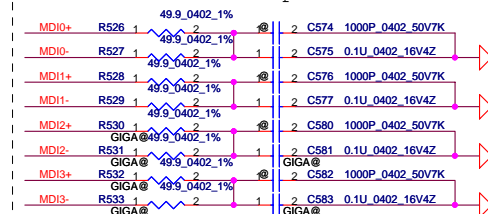
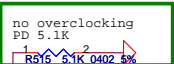
Reserve for SW mini-pcie debug card.  
Series resistors closed to KBC side.

LPC_FRAME#_R	R508	1	2	0.0402 5%	LPC_FRAME#	LPC_FRAME# <14,32>
LPC_AD3_R	R509	1	2	0.0402 5%	LPC_AD3	LPC_AD3 <14,32>
LPC_AD2_R	R510	1	2	0.0402 5%	LPC_AD2	LPC_AD2 <14,32>
LPC_AD1_R	R511	1	2	0.0402 5%	LPC_AD1	LPC_AD1 <14,32>
LPC_AD0_R	R512	1	2	0.0402 5%	LPC_AD0	LPC_AD0 <14,32>
PCI_RST#_R	R513	1	2	0.0402 5%	BUF_PLT_RST#	BUF_PLT_RST# <18>
CLK_PCIE_DB					CLK_PCIE_DB	CLK_PCIE_DB <15>

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				Size	Document Number
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Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable *	H
LED2	H:SWR Switch mode regulator Select* AR8151 Pin23=LED2. AR8152, Pin23 is CLKREQ	--



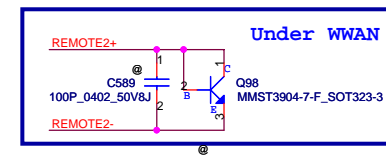
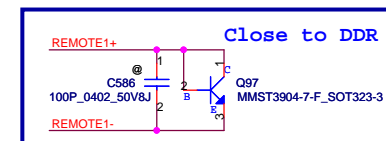
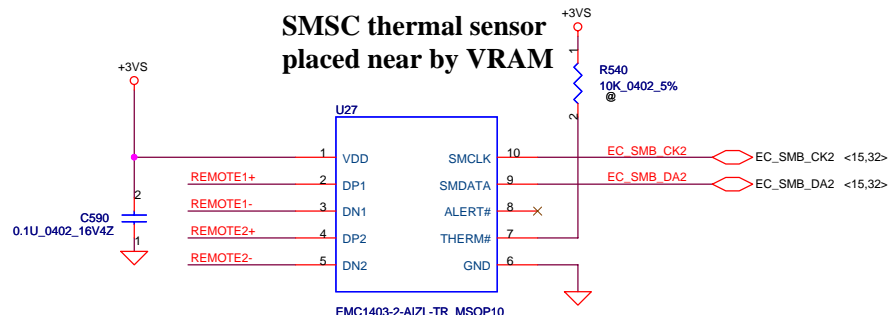
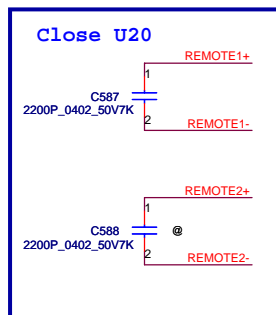
```
| Note 1 : 8152 no mount MDI3+, MDI3-, MDI2-, MDI2+
| resister and cap
```

Note 2 : C574, C576, C580, C582, reserved for EMI.

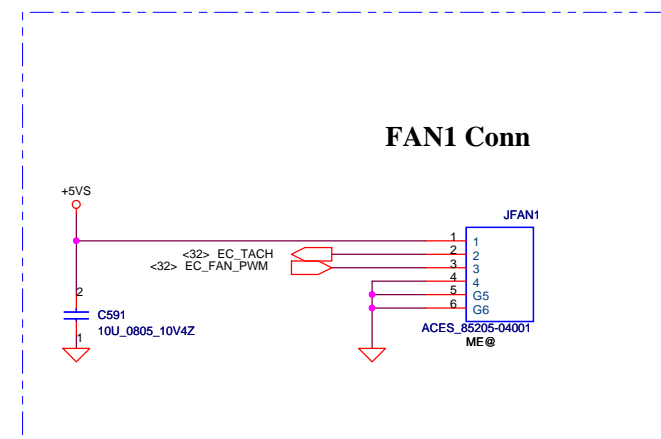
	Pin4	Configure			Pin23	Configure
		R525	C559			
AR8152	VDDCT_REG		*		CLKREQn	*
AR8151	CLKREQn	*			LED[2]	

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Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title		
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				Size	Document Number	Rev
				Custom	LA-675AP	1.0
Date:				Thursday, May 05, 2011	Sheet	27 of 51



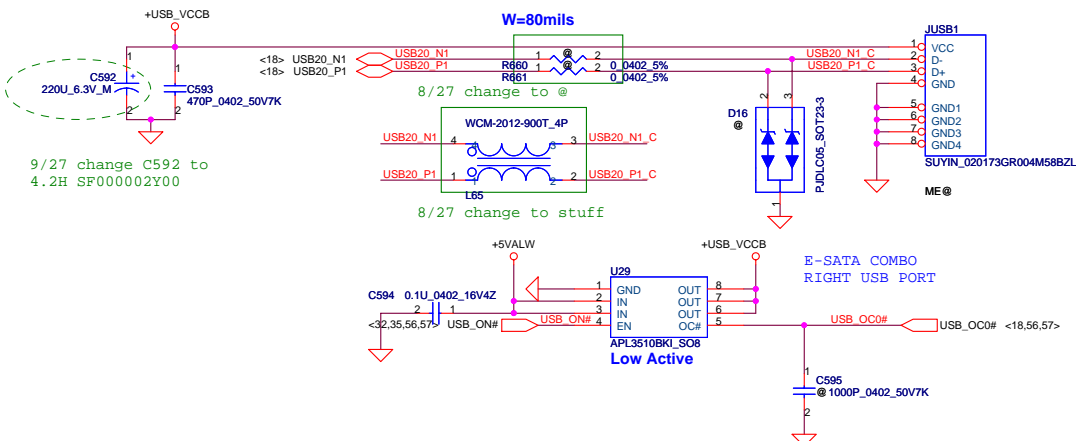


REMOTE1,2+/-:  
Trace width/space:10/10 mil  
Trace length:<8"

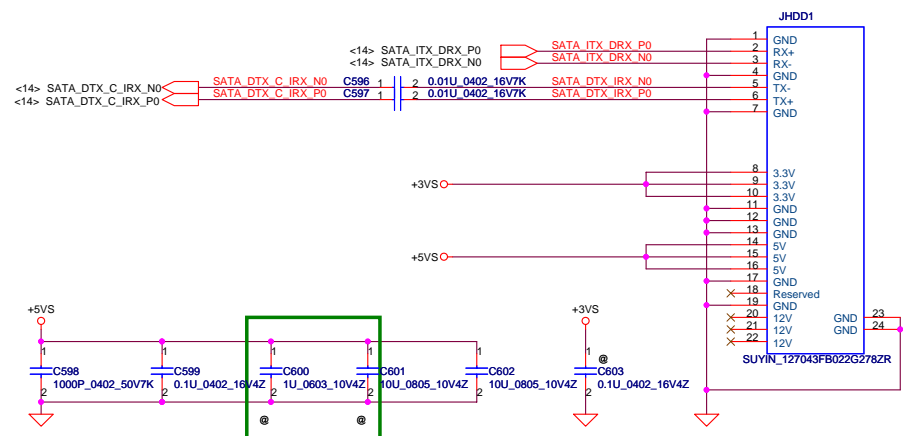


Security Classification		Compal Secret Data		Compal Electronics,Ltd.	
Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title	EMC1403_Thermal sensor/FAN
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				Date: Thursday, May 05, 2011	Rev 1.0
				Sheet 29 of 51	

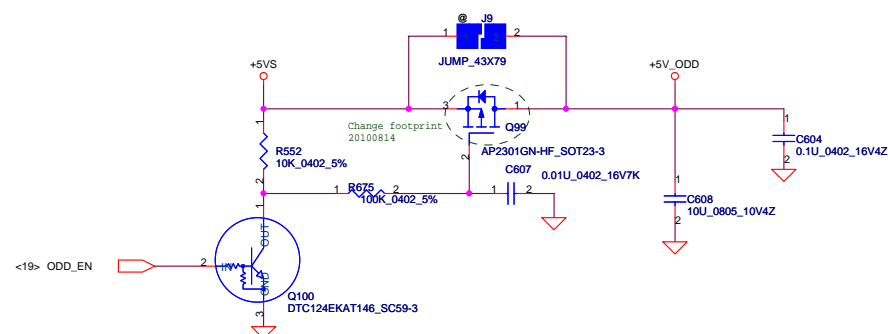
## Left USB Conn.



## SATA HDD Conn.

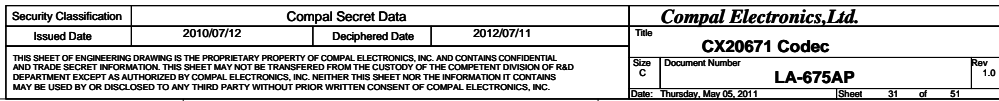
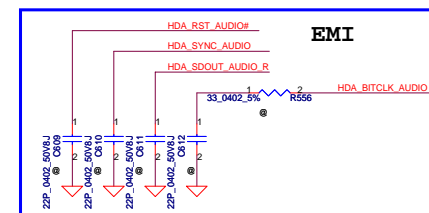


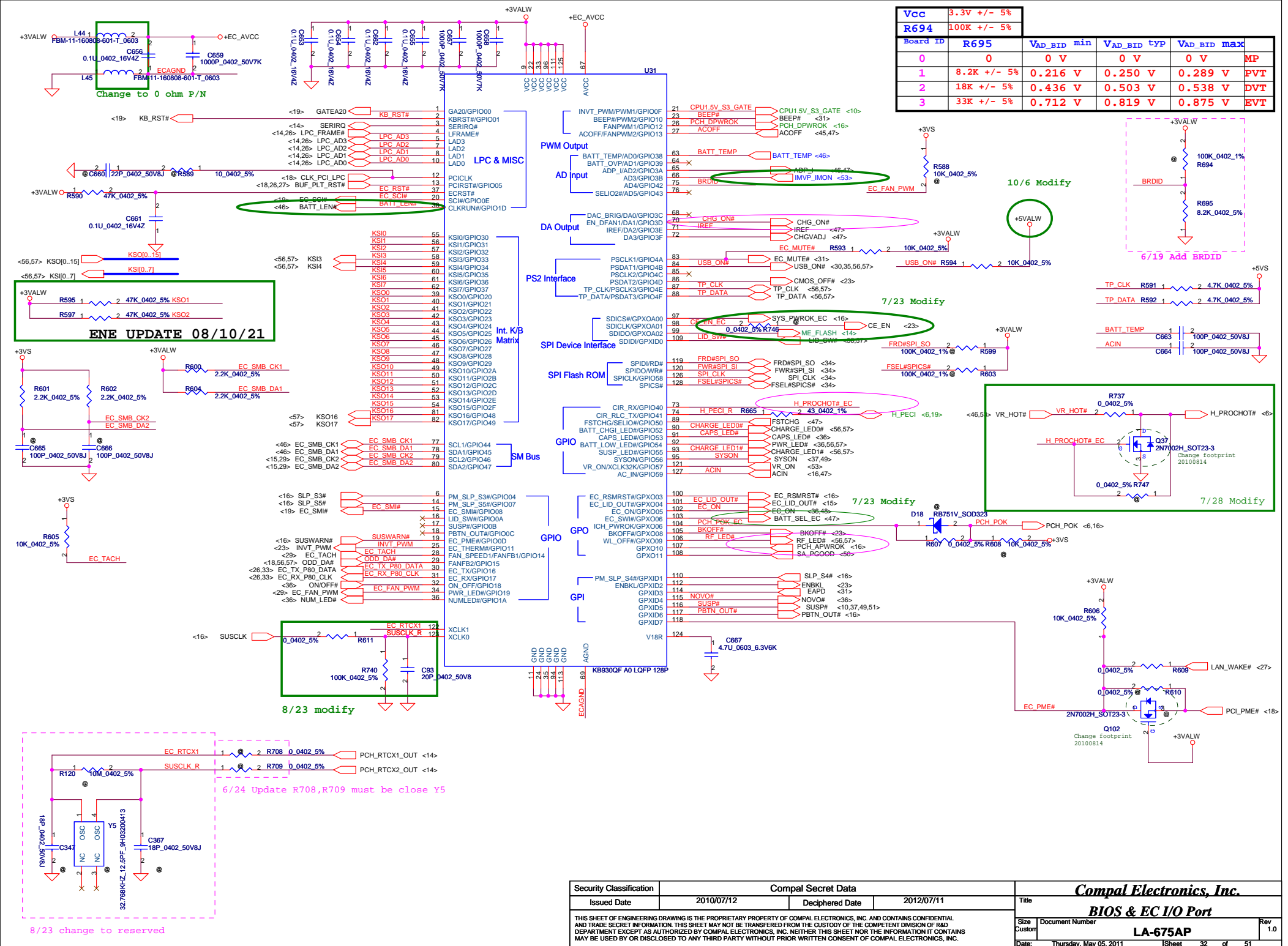
## ODD Power Control



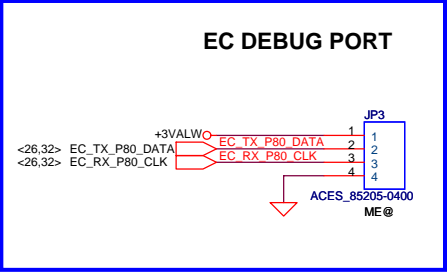
Security Classification	Compal Secret Data			Title		
Issued Date	2010/07/12	Deciphered Date	2012/07/11	Compal Electronics, Inc.		
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				Size B	Document Number	Rev 1.0
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				Date:	Thursday, May 05, 2011	Sheet 30 of 51

9/27 Update U30 P/N to SA00003K410



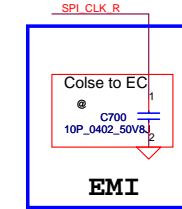
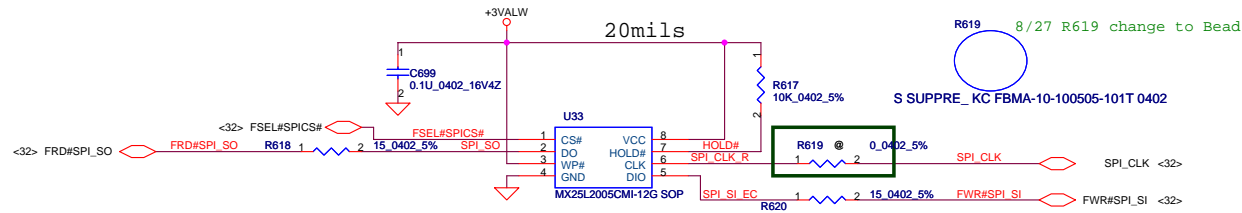


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Issued Date	2010/07/12	Deciphered Date	2012/07/11	<b>BIOS &amp; EC I/O Port</b> Title		
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				Custom	LA-675AP	1.0
				Date:	Thursday, May 05, 2011	ISheet 32 of 51

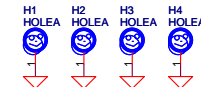


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Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title	KB /SW /LPC Debug Conn.
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FOR EC 128KB SPI ROM  
(150mil PACKAGE)  
SA00003FL10  
SA00003JD00



H\_3P8



H\_3P3



H\_3P0x4P5N



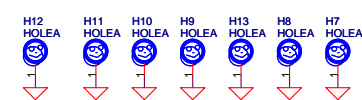
H\_3P0N



H\_6P0



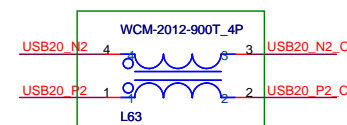
H\_2P8



Security Classification	Compal Secret Data			Title	
Issued Date	2010/07/12	Deciphered Date	2012/07/11	LED/EC SPI ROM	
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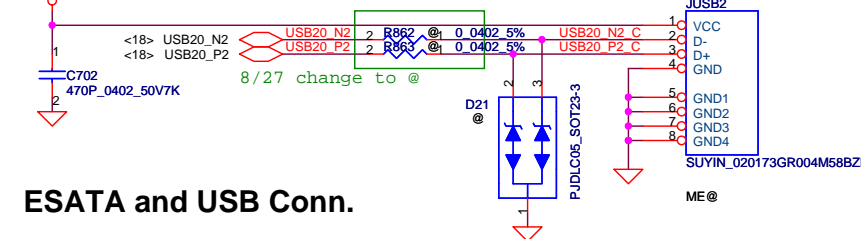
(220uF\_6.3V\_5.9L\_ESR17m)\*2=(SF000001500)

8/27 change to stuff



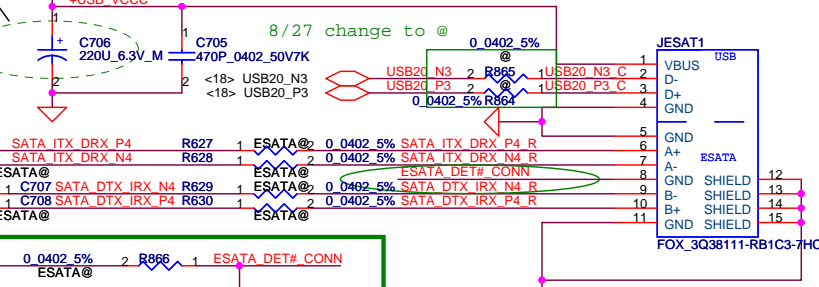
### Left USB Conn.

+USB\_VCC W=80mils

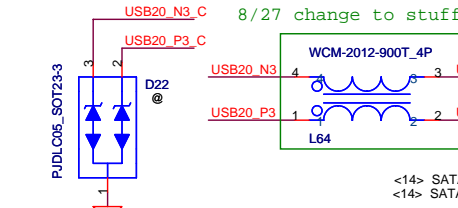
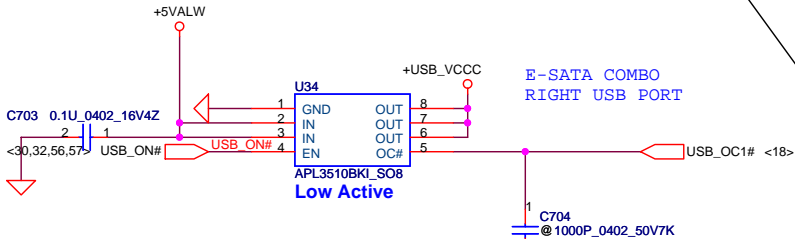


### ESATA and USB Conn.

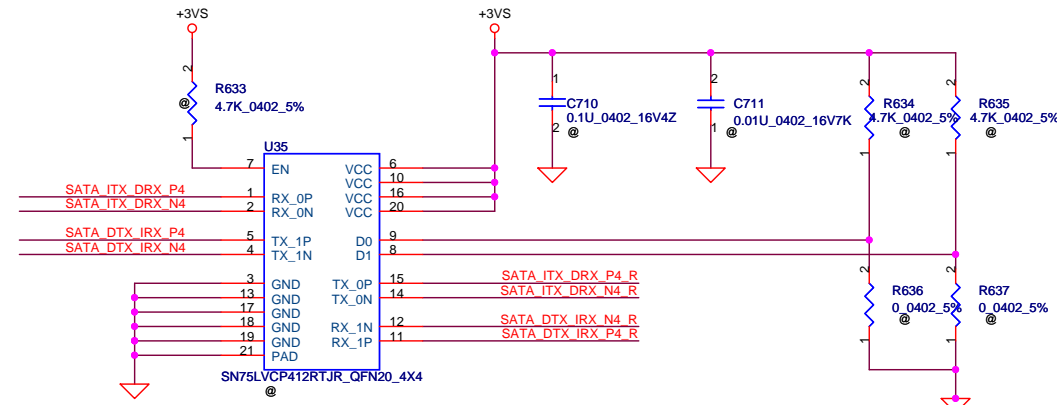
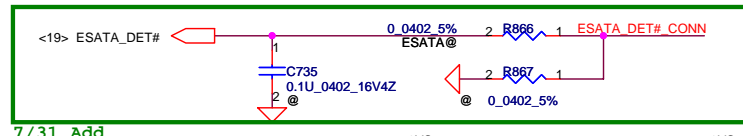
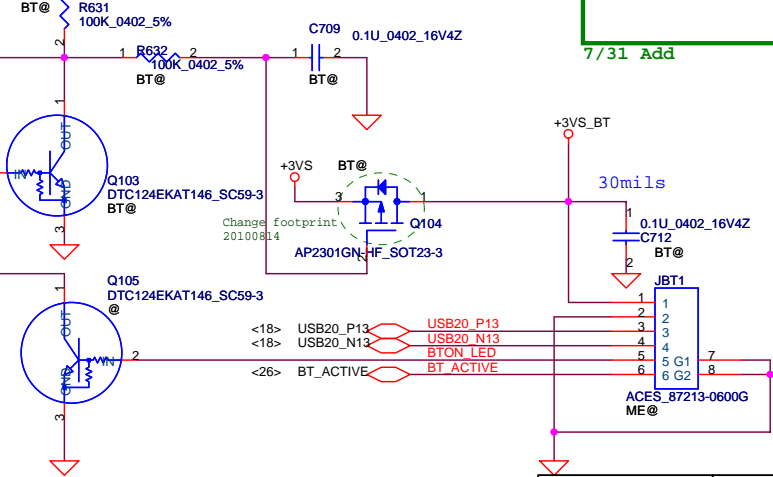
+USB\_VCC W=80mils



**USB**  
A+ = RXP  
A- = RXN  
B- = TXN  
B+ = TXP

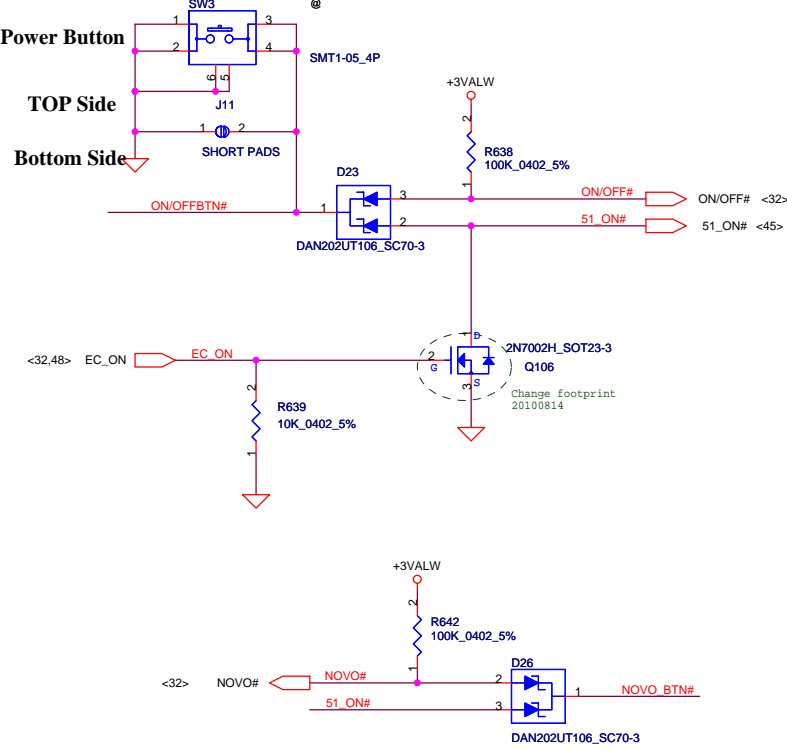


### BT MODULE CONN

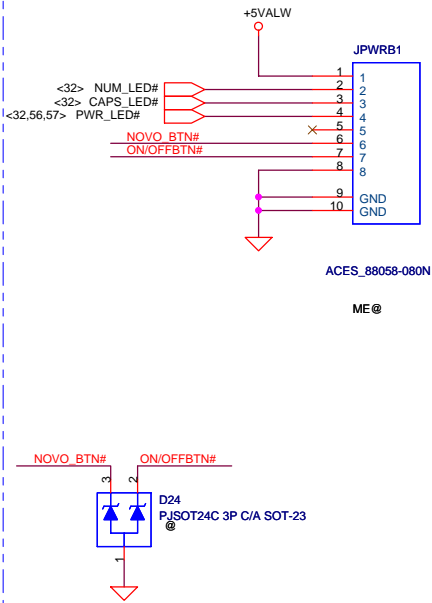


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Issued Date		2010/07/12		Deciphered Date		2012/07/11		Title						
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								Size	Document Number			Rev		
								Custom	LA-675AP			1.0		
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ON/OFF switch

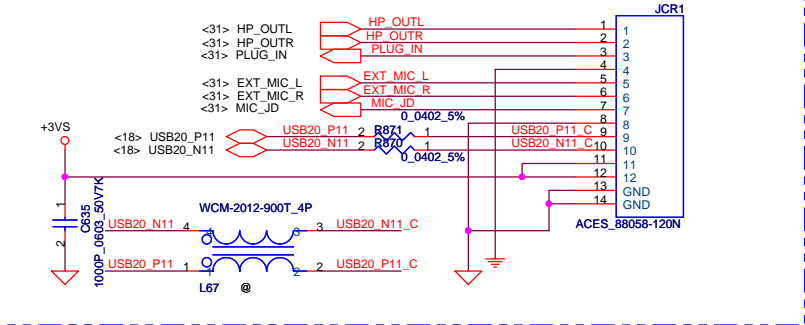


Power Bottom Board Conn. 8pin

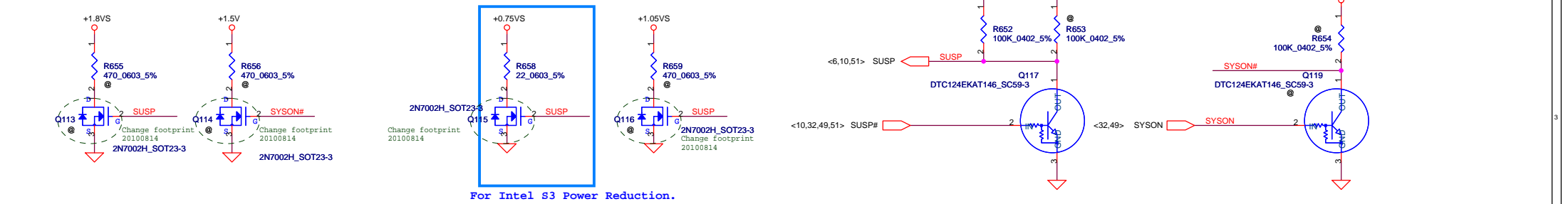
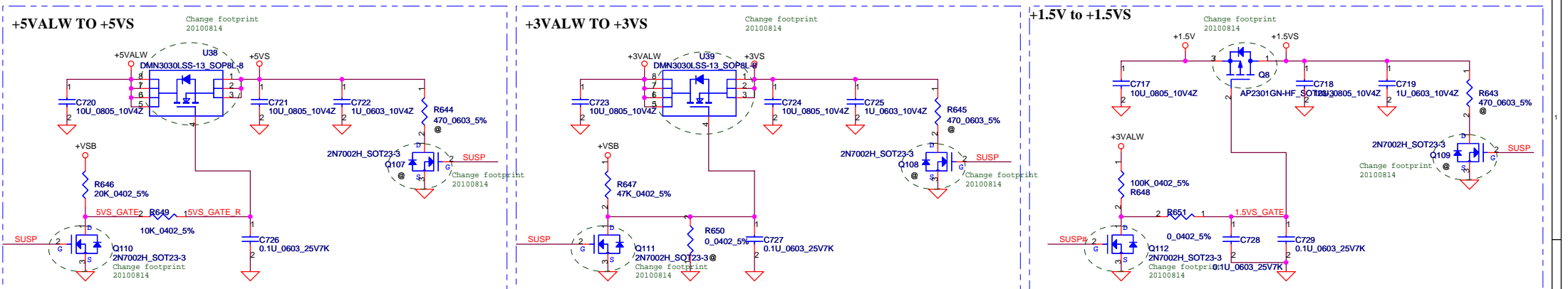


EMI REQUEST 1ST = SCA00000E00  
2ST = SCA00000R00

Card Reader/Audio Jack SB CONN

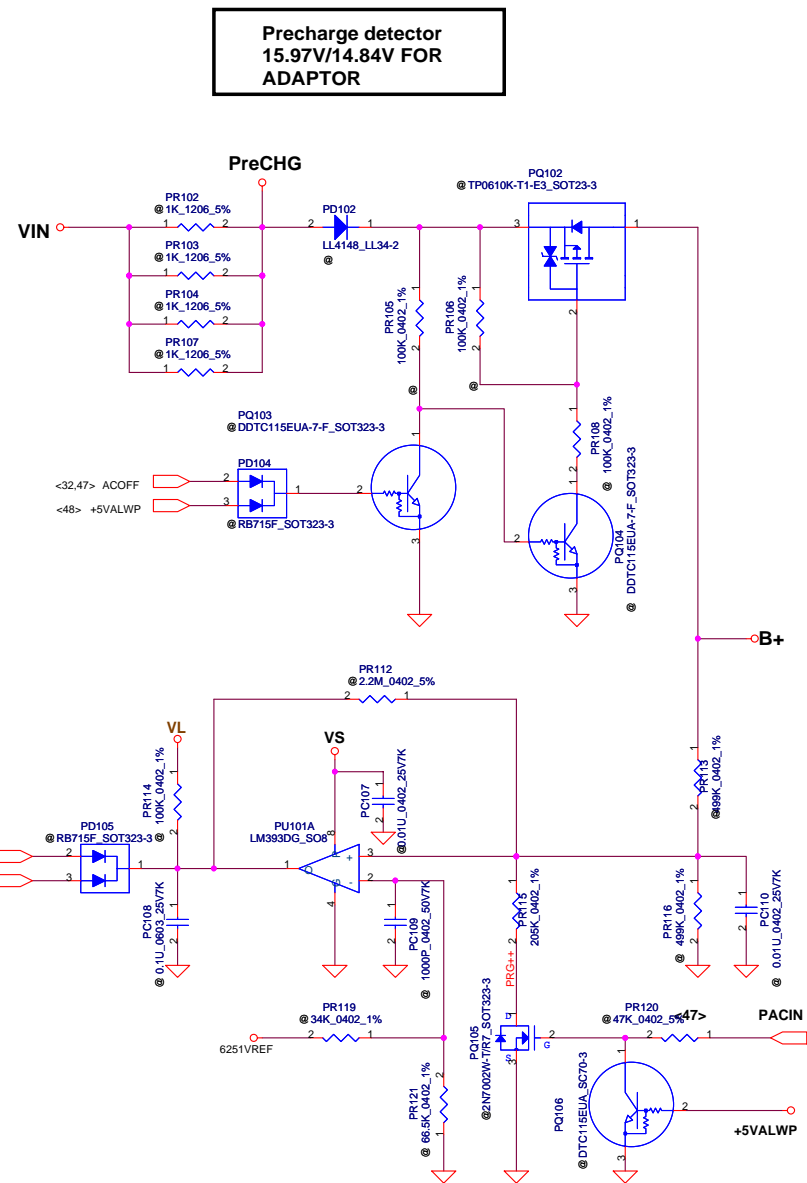
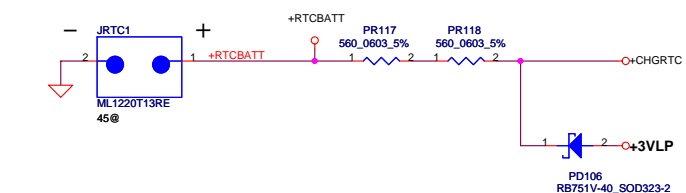
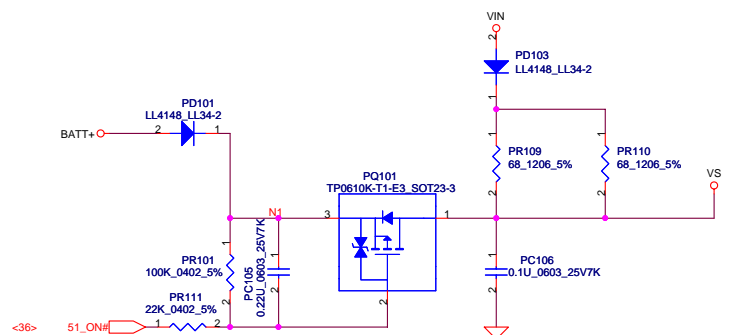
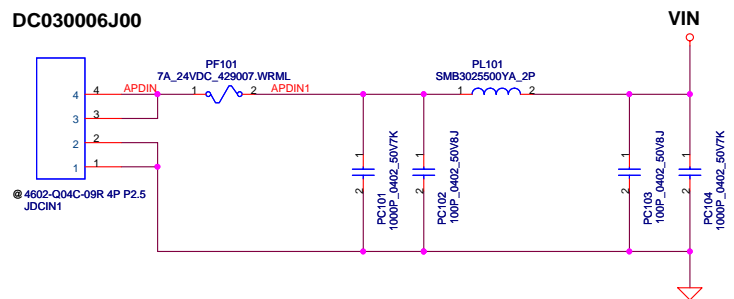


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For Intel S3 Power Reduction.

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				Custom	LA-675AP	1.0
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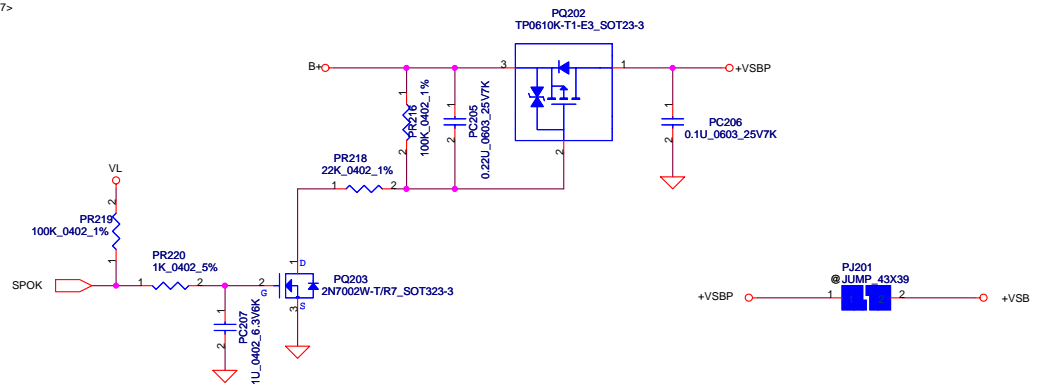
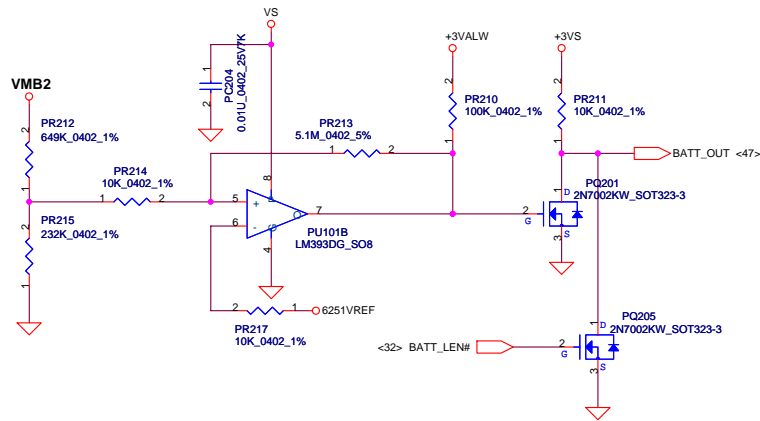
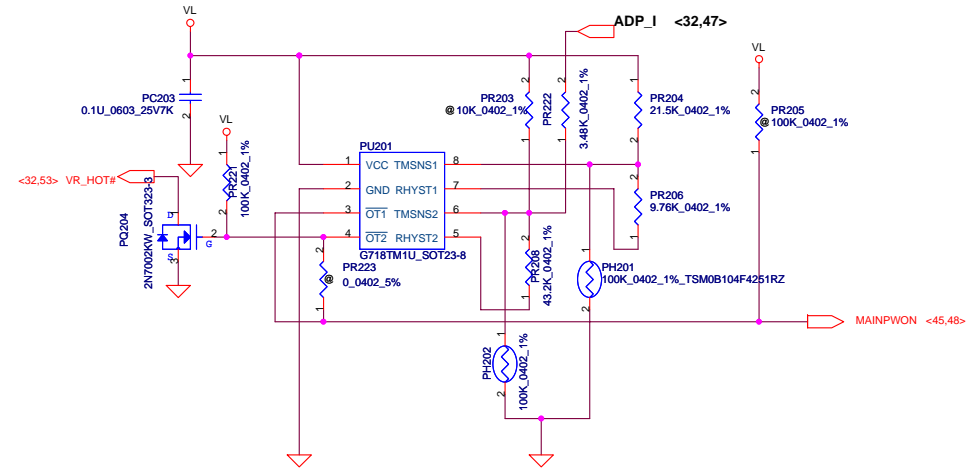
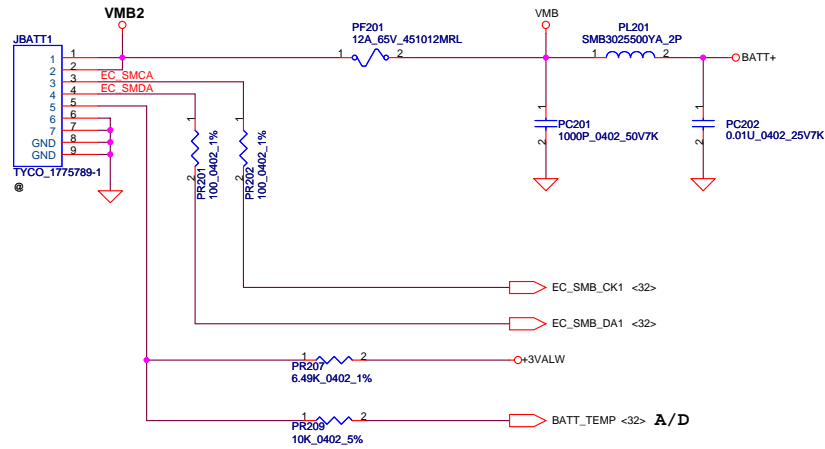


	Precharge detector		
	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

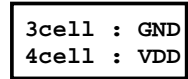
BATT ONLY			
	Precharge detector		
	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

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PH201 under CPU botten side :  
CPU thermal protection at 92 degree C  
Recovery at 56 degree C



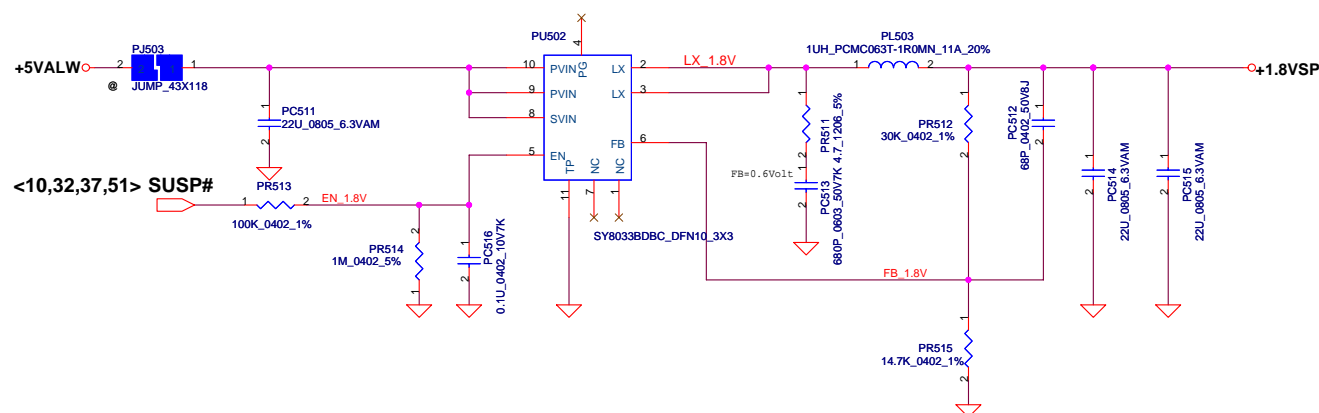
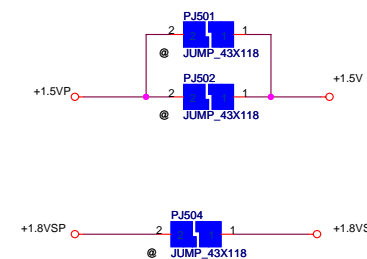
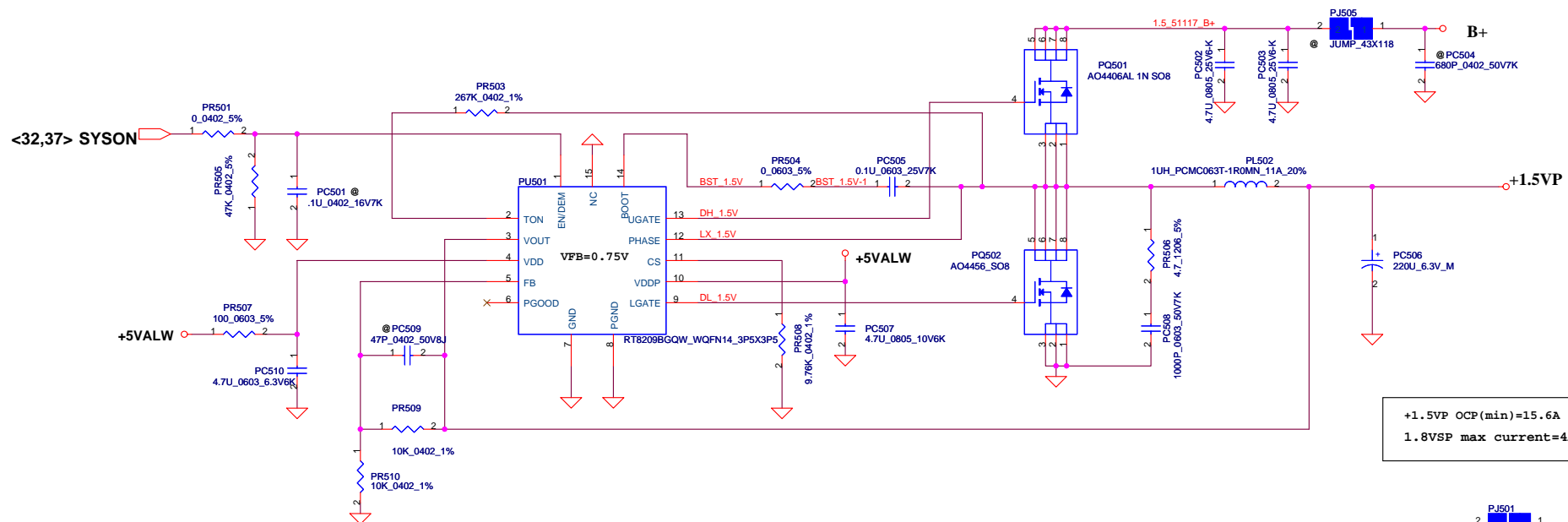
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				PWR-BATTERY CONN/OTP					
				Size		Document Number		Rev	
				Custor		LA-675AP		1.0	
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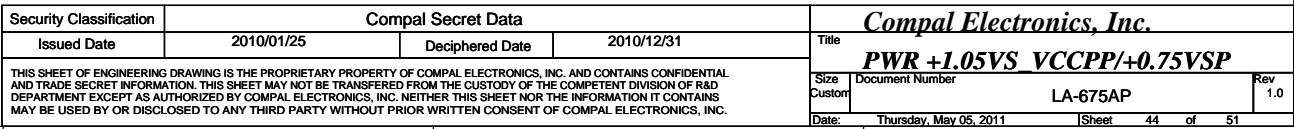
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+3.3VALWP OCP(min)=5.81A +5VALWP OCP(min)=8.44A
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Customer					1.0
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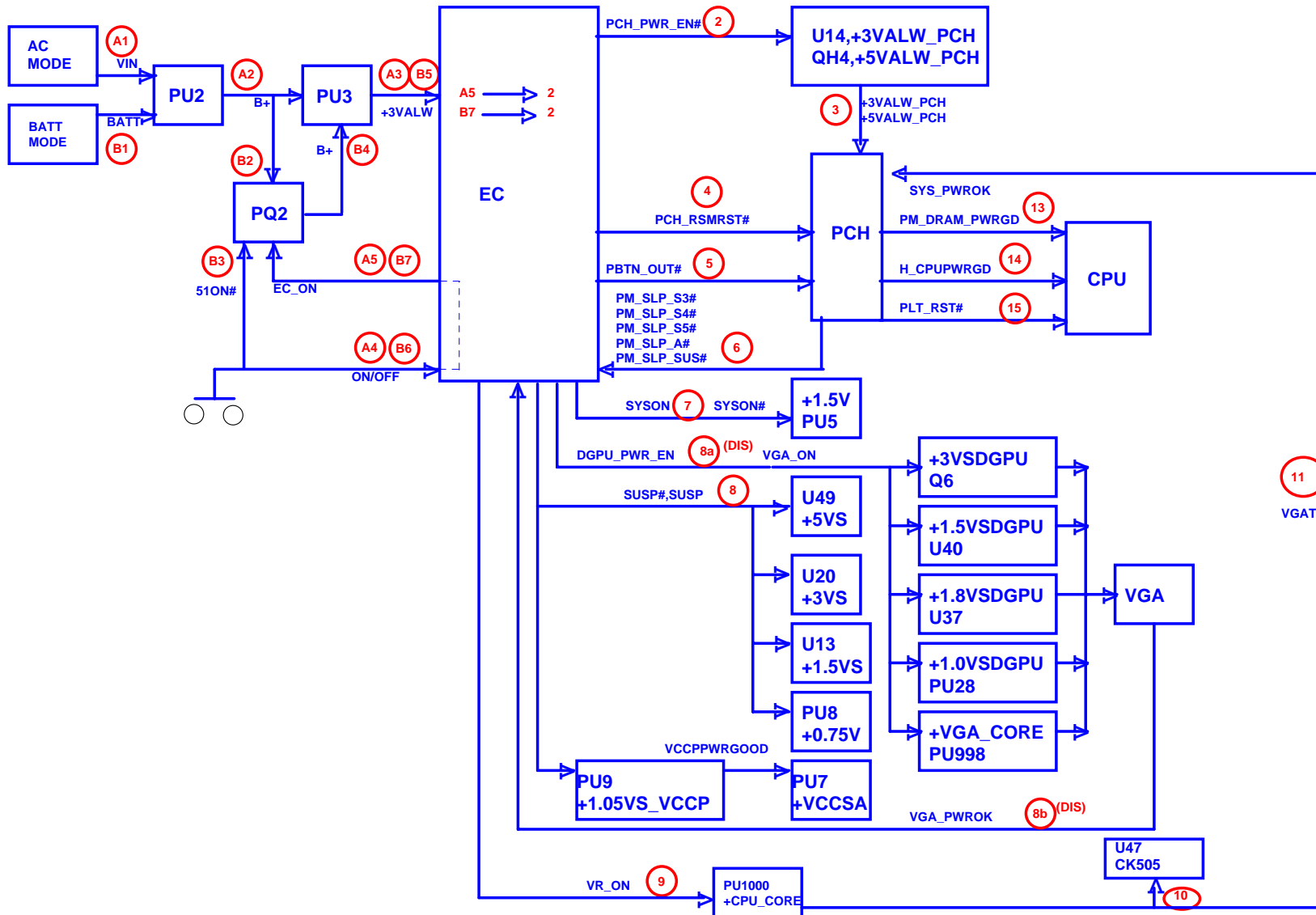
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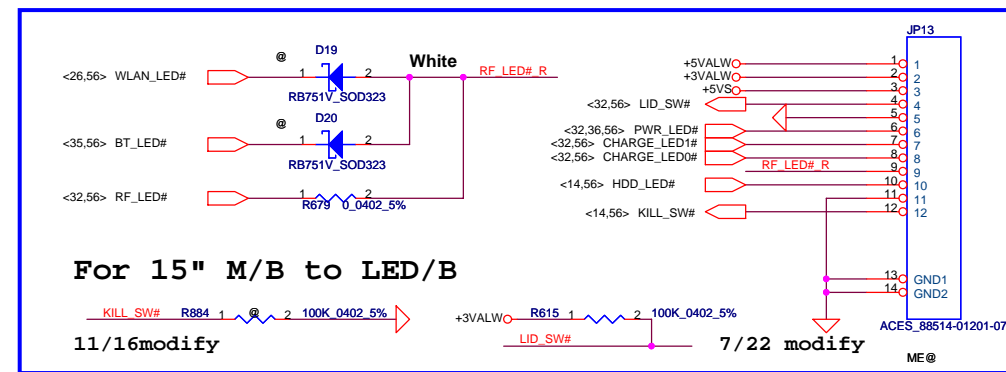
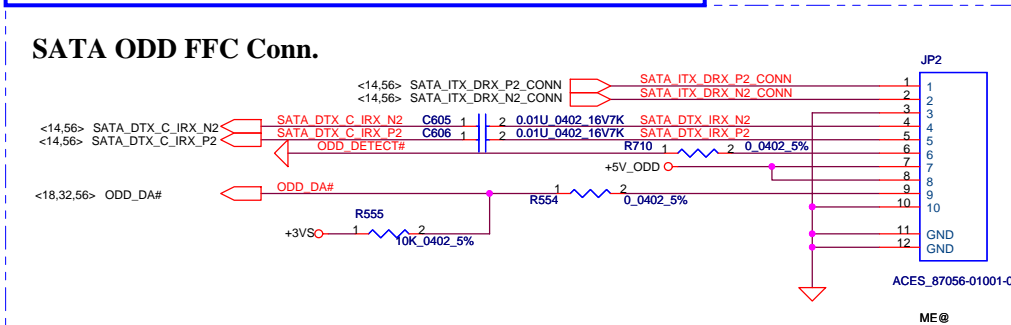
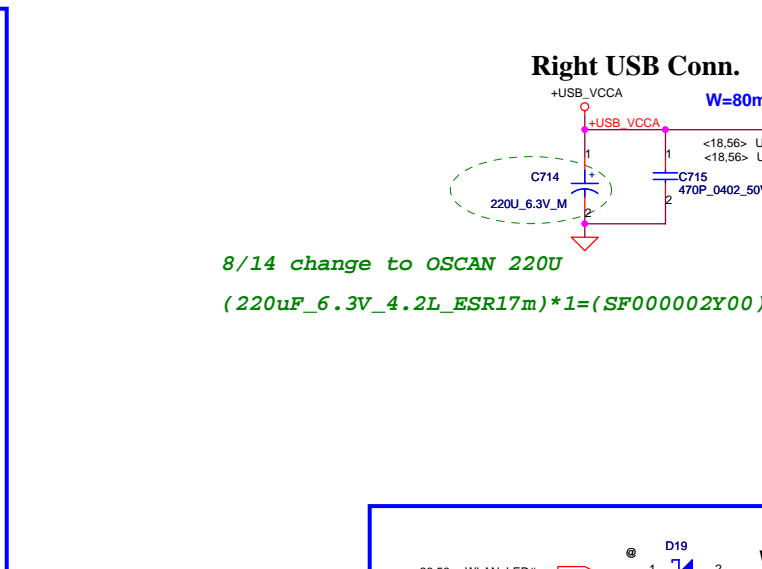
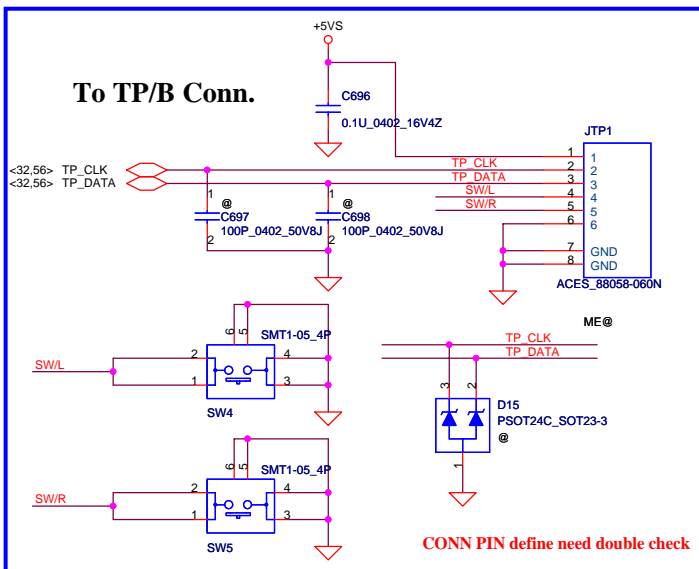
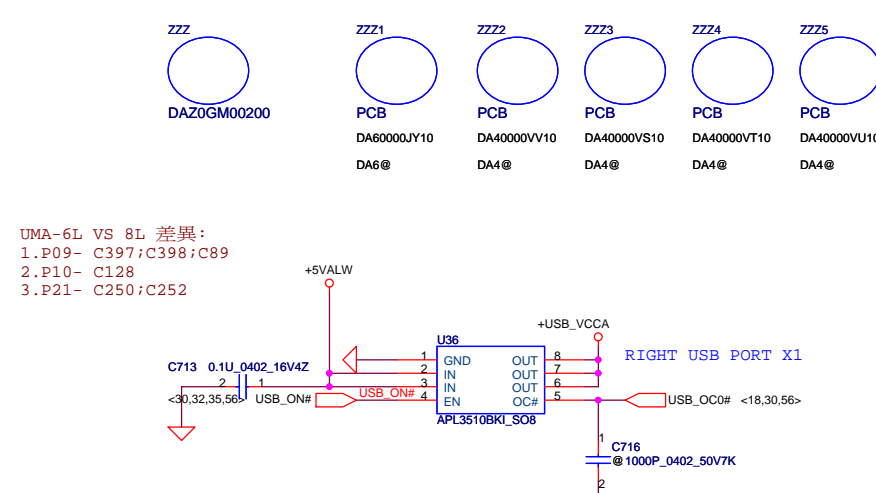
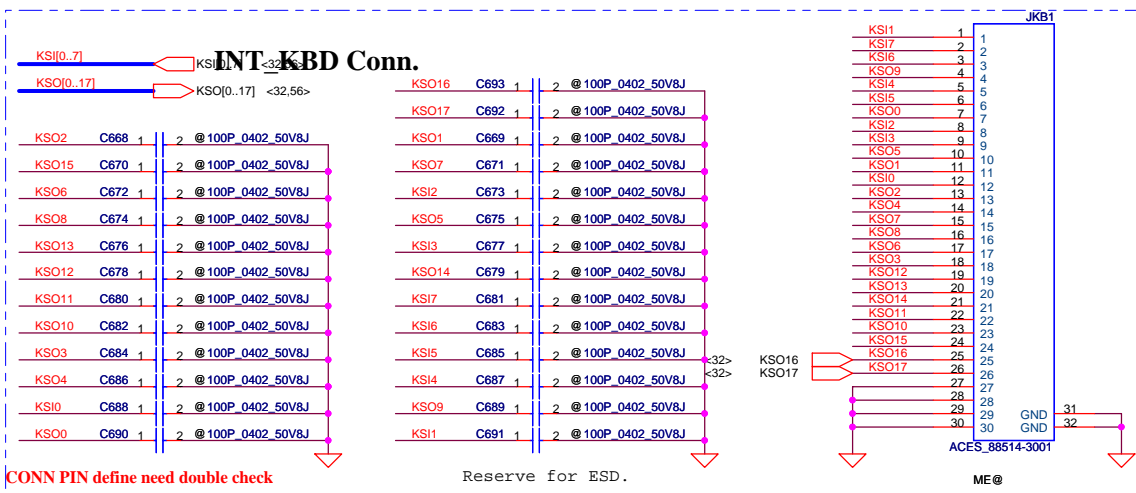
\*OCP setting value=37A

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Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
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15					
16					
17					

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Security Classification		Compal Secret Data		Title	
Issued Date	2010/07/12	Deciphered Date	2012/07/11	KB /SW /LPC Debug Conn.	
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	5		4		3		2		1
	PHASE	PAGE	Modification list			PURPOSE			
	0.2	P31	Change CRT Symbol			For CRT footprint issue			
	0.2	P31	Del C510			For Non-used part			
	0.2	P39	change C610 pin 1 net name			change C610 pin 1 net name to correct			
	0.2	P35	U25 change to U26			For co-lay 10/100 and GIGA			
	0.2	P40	Add R740, C93			For EC request			
	0.2	P18	Change R215 pin1 net name			Change R215 pin1 net name to correct			
	0.2	P16	Add R742, R743			For PCH power sequence			
	0.2	P38	Del U28, R542-R551, J12			Del USB charger circuit			
	0.2	P40	Add EC pin 97,98,103			Add EC pin 97 for SYS_PWROR_EC, pin 98 for CE_EN, pin 103 for BATT_SEL_EC			
	0.2	P39	Change J10 footprint and Add J13			Change J10 footprint by DfX request and Add J13 by vendor suggestion			
	0.2	P39	Change PC_Beep circuit			Change PC_Beep circuit			
	0.2	P6	Add R161,			Follow ORB circuit			
	0.2	P58/59	Add R615 in 15" and 17" page			Pull high LID_SW# at M/B side			
	0.2	P31	Add Q83 pin 1 power net name +CMOS_PW			For power trace net			
	0.2	P56/57/58	Change JP21 to JKB1			Change connector to standard name			
	0.2	P56/57/58	Change JP4 to JTP1			Change connector to standard name			
	0.2	P43/60	Change JP6 to JPWRB1			Change connector to standard name			
	0.2	P34	Change JP1 to JWLN1			Change connector to standard name			
	0.2	P42	Change JP5 to JBT1			Change connector to standard name			
	0.2	P43/60	Change JP7 to JCR1			Change connector to standard name			
	0.2	P19	Add R542			For ESATA detect function			
	0.2	P42	Add R866, R886, C735			For ESATA detect function			
	0.2	P31	Add R543			For reserve EC control directly			
	0.2	P39	Change J10 footprint, Del C635, C636			Change J10 for DfX and Del component for layout			
	0.2	P42	Add R877			For reserve EC control directly			
	0.2	P42	SW3 BOM structure change to @			For ME ASSY concern			
	0.2	P42	Change ESATA from port 5 to port 4			For intel risk			
	0.2	P15	Add R544,R545			For Pull high SMBus			
	0.2	P12/13	Del R74-R80,R82 R88-R94,R96			For DDR3 DM Bus to GND			
	0.2	P16	Add R182,R546			Add 186 for reserve sequence, Add R546 for follow CRB & ORB			
	0.2	P20	Del Add J12, R257 change to @			For voltage drop			
	0.2	P6	R161 change to I00K			Follow CRB			
	0.2	P19	Add R547, R250 change to @			Follow Module and CRB			
	0.2	P18	WLAN USB port for port8 to port9			For debug port			
	0.2	P39	Del J13			For layout space			
	0.2	P20,39,42	Add C395, R581, R583, R584, R586, R587			For customer request reserved			
	0.2	P20	Add C129, C396, Del R264			For reserved			
	0.2	P40	Add PIN 66, R740,C93 change to @			Add IMVP_IMON			
	0.2	P9	Add R74			For VCCIO_SENSE / VSSIO_SENSE differential routing			
	0.2	P30	Del R419~425, R427~R429			Del 0 ohm for UMA only			
	0.2	P31	Del R439, R440, R441			Del 0 ohm for UMA only			
	0.2	P32	Del RQ51 ~ Q54 Add Q95			For DIS HDMI			
	0.2	P38	Del J10, C637,C640,R576,R577,R579 change to @, L40~L43 change to R720~R723			For Vendor suggestion and EMI			
			Del C643, R578, MIC_INR connect MIC_INL, Add R578			Del C653, R578 connect MIC_INR/L for vendor suggestion, Add R578 for EMI			
	0.2	P20	Add L75, R264, C917, R259 C226 change to @			For intel PDDG update			
	0.2	P43	C714 change to OSCON CAP			C714 change to OSCON CAP			
	0.2	P9	Add C394, C397, C398, C399, Add R75			For CPU_CORE power reserved at Bottom side, Add R75 for reserved at cpu side and pwr side			
	0.2	P42	Change C706 F/N to SF000001500			Change to H=6 OSCAN			
	0.2	P10	Change C128 to @			For Reserved			
	0.2	P56	Update JODDI symbol			For ME update drawing			

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				Size B	Document Number
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PHASE	PAGE	Modification list	PURPOSE
0.2	P16	D29 change to @	For AC detect issue
0.2	P24	R548,R549 change to DIS@	For AC detect issue
0.2	P10	C128 change to stuff	For test on DVT
0.2	P44	Del Q118, R657	For not need
0.2		Change R513, R516 ,R667 P/N and from 0805 to 0603	For common part
0.2		Change C633, C634 , C642	For common part
0.2		Change D3, D29 P/N and symbol	For common part
0.2		Change U3,U11,U13,U14,U38,U39 P/N and symbol	For common part
0.2		Change U3,U11,U13,U14,U38,U39 P/N and symbol	For common part
0.2		Change Q8,Q65,Q80,Q83,Q99,Q104 P/N and symbol	For common part
0.2		Change Q1,Q37,Q93 P/N and symbol	For common part
0.2		Change Q94, Q95 P/N and symbol	For common part
0.2		Change Q3,Q4,Q7,Q9,Q66,Q67,Q68,Q73,Q74,Q75,Q76,Q77,Q78, Q79,Q82,Q85,Q86,Q87,Q102,Q106,Q107,Q108,Q109,Q110,Q111,Q112,Q113,Q114,Q115,Q116 P/N and symbol	For common part
0.2		Change C635 part and change to @	For EMI
0.2	P18	Reserved R297	Reserved
0.2	P9	Change C53,C85,C86,C87 ,C397,C398,C399 to stuff and change ,C48,C80,C81,C82, C90,C91 to @ Del C89	For CPU_CORE
0.2	P10	Change C110,C111,C112,C113 to stuff	For VGFX_CORE
0.2	P56	Change LED1/LED3/LED4 P/N to SC50000A300	Change P/N
0.2	P36	Change T1,T2 P/N to SP0500003N00	For test pass part
0.2	P40	Change R611,R740,C93 to stuff and change Y5,C347,C367 to @ Change R695 to 18K, Q37 change to @, R747 change to stuff,	For SUS_CLK R695 for Board ID, Q37, R747 for VR_HOT
0.2	P40	Change U33 P/N to SA00003PL10	For BIOS ROM
0.2		Change C509,C511,C635 to stuff	For EMI
0.2	P56	Change I4,C714 P/N to SGA00002N80	For Sourcer request
0.2	P39	Change R720,R721,R722,R723 P/N to SM01000BZ00(Bead), and Change C647,C649,C650,C651 to Stuff	For EMI request
0.2	P19	Change R303 to Stuff, and change R542 to @	For BIOS ESATA detect function
0.2	P56	Change U32 P/N to SA000031C00	For common part
0.2	P36	Change T1,T2 P/N to SP0500006E00	For correct part
0.2	P10	R688 change to stuff , R687 ,Q7 change to @	For S3 power reduction
0.2		Change R660,R661,R862,R863,R864,R865,R868,R869 to @ , change L63,L64,L65,L66 to stuff , change R619 to Bead (SM01000DI00)	For EMI
0.2	P20	Change L75 symbol	For common part
0.2	P30	Change R402 to @	For DPST
0.3	P10	Update Q5 symbol	For update symbol
0.3	P33	Add F2	For safty request
0.3	P39	Update U30 P/N to SA00003K410 and Add R879	For Audio update to 21Z
0.3	P10	Change C128 to D2 size and @	Change size for M/E issue
0.3	P14	Add reserve R878	For Intel DG 1.5
0.3	P37	C592 change P/N to SP000001500 (H=6)	For ME Z high ok
0.3	P29	R369 P/N change to SD034I00A80	For GP part
0.3	P6	Reserved R880 to SYS_PWR0K	Follow ORB
0.3	P10	R62,R63 change to 1K	Follow CRB
0.3	P33	R483,R484 change connect to +5V_HDMI_F	For Add F2
0.3	P37	Change U27 P/N to SA000046C00	For Fintek
0.3	P40	Change R594 pull high to +5VALW	For leakage issue

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	5		4		3		2		1
PHASE	PAGE	Modification list				PURPOSE			
0.3	P19	R881 change to Dtuff, R244 change to @				For intel MRC Rev0.9			
0.3	P14	R878 change to stuff				For intel DG 1.5			
0.3	P31	Del R432				For non-used part			
0.3	P36	Reserved D31 , C643 , C644				For reserved EMI parts			
0.3	P37	Del R581				For non-used part			
0.3	P38	Del R550				For non-used part			
0.3	P38	Change C592 P/N to SF000002Y00				For M/E Z high limlt			
0.3	P39	Del R584, R586 , R587				For non-used part			
0.3	P40	Change R600, R604 to 2.2K Change R695 to 8.2k				Change R600, R604 for Battery SMBus, R695 for Board ID			
0.3	P42	Del R583				For non-used part			
0.3	P31	Del R449, R452, R458, R460 (UMA change only)				For non-used part			
0.3	P32	Del R478, R480, R486 (UMA change only)				For non-used part			
0.3	P6	Reserved R882 connect to PCH_PWROK				Reserved for intel			
0.3	P56	R765 change to 300 ohm				For LED			